

TANDY®

ServiceManual

26-3803

Tandy 102 PORTABLE COMPUTER

Catalog Number: 26-3803



CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

CONTENTS

PART I. INTRODUCTION	1-1
System Overview	1-2
External View	1-2
Internal View	1-5
Specifications	1-7
 PART II. DISASSEMBLY INSTRUCTIONS.....	 2-1
Cases	2-1
Keyboard and LCD PCBs.....	2-1
Main PCB.....	2-2
 PART III. MAINTENANCE.....	 3-1
To clean the body and LCD display	3-1
 PART IV. THEORY OF OPERATION.....	 4-1
General.....	4-1
Block Diagram	4-2
CPU.....	4-3
Memory	4-3
I/O Map	4-5
Keyboard	4-6
Cassette Interface Circuit	4-7
Printer Interface Circuit	4-8
Bar Code Reader Interface Circuit	4-9
Buzzer Control Circuit.....	4-10
System Bus	4-11
Clock Control Circuit	4-12
Serial Interface Circuit.....	4-14
LCD	4-21
Power Supply Circuit	4-24
 PART V. TROUBLESHOOTING	 5-1
General Guidance	5-1
Troubleshooting Guide	5-1
Check List	5-11

PART VI. EXPLODED VIEW/PARTS LIST	6-1
Electrical Parts List	6-2
Mechanical and Assembly Parts List	6-11
 PART VII. SCHEMATIC DIAGRAMS/PCB VIEWS	 7-1
Schematic Diagrams.....	7-1
PCB Views.....	7-3
 APPENDIX A/ INSTALLATION	 A-1
Installation of Optional RAM and ROM	A-1
 APPENDIX B/ KEYBOARD LAYOUT, CONNECTOR PIN	
ASSIGNMENTS AND CHARACTER CODE TABLE.....	B-1
B-1. Keyboard Layout.....	B-1
B-2. Connector Pin Assignments	B-2
B-3. Character Code Table.....	B-7
 APPENDIX C/ TECHNICAL INFORMATION	 C-1
C-1. 80C85A	C-1
C-2. 81C55.....	C-7
C-3. 6402	C-13
C-4. Basic Construction of LCD	C-19

List of Illustrations

FIGURE NUMBER	DESCRIPTION	PAGE NUMBER
1-1	Front View.....	1-2
1-2	Rear View	1-3
1-3	Bottom View	1-4
1-4	Main PCB (Bottom View).....	1-5
1-5	LCD PCB	1-6
2-1	Top Case Removal	2-1
2-2	Keyboard and LCP PCBs Removal	2-1
2-3	Main PCB Removal.....	2-4
4-1	Organization of Section IV	4-1
4-2	System Block Diagram	4-2
4-3	Functional Block Diagram of Bus Separation Circuit.....	4-3
4-4	Memory Map	4-3
4-5	Address Decoding and Bank Selection Circuit	4-4
4-6	I/O Address Decoding Circuit.....	4-5
4-7	Condition of Pressing "T" Key	4-6
4-8	Cassette Interface Circuit.....	4-7
4-9	Printer Interface Circuit	4-8
4-10	Bar Code Reader Interface Circuit	4-9
4-11	Buzzer Control Circuit	4-10
4-12	Time Set Sequence of μ PD1990AC.....	4-12
4-13	Time Read Sequence of μ PD1990AC	4-13
4-14	Functional Block Diagram of the Serial Interface	4-14
4-15	RS-232C/MODEM Selection Circuit.....	4-15
4-16	RS-232C Interface Circuit	4-16
4-17	MODEM IC and Peripheral Circuit.....	4-17
4-18	Transmission Filter Circuit	4-17
4-19	Reception Filter Circuit.....	4-18
4-20	MODEM Adjustment.....	4-19
4-21	MODEM Connector Interface Circuit	4-20
4-22	HD44103 Internal Logic Diagram	4-21
4-23	HD44102 Internal Logic Diagram	4-22
4-24	LCD Waveform.....	4-23
4-25	Power Supply and Reset Circuit	4-25
6-1	Exploded View	6-1
7-1	Main PCB – Schematic Diagram.....	7-1
7-2	LCD PCB – Schematic Diagram	7-2
7-3	Main PCB – Top View	7-3
7-4	Main PCB – Bottom View.....	7-4
7-5	LCD PCB – Top View	7-5
A-1	Installation of RAM and ROM.....	A-1
B-1	Keyboard Layout	B-1
B-2	System Bus Connector.....	B-2
B-3	RS-232C Connector	B-3
B-4	Printer Connector	B-4
B-5	Cassette Connector.....	B-5
B-6	MODEM Connector	B-5
B-7	Bar Code Reader Connector	B-6
C-1	Functional Block Diagram.....	C-1
C-2	Pin Configuration of 80C85A	C-1
C-3	Trap and RESET IN	C-5
C-4	80C85A Basic System Timing	C-7
C-5	Functional Block Diagram.....	C-7

FIGURE NUMBER	DESCRIPTION	PAGE NUMBER
C-6	Pin Configuration of 81C55.....	C-7
C-7	Internal Register of 81C55	C-9
C-8	Programming the Command/Status Register	C-10
C-9	Reading the C/S Register.....	C-11
C-10	Bit Assignments to the Timer Counter	C-11
C-11	Functional Block Diagram.....	C-13
C-12	Pin Configuration of 6402.....	C-13
C-13	Receiver Timing	C-16
C-14	Transmitter Operation	C-17
C-15	Start Bit Detection Timing	C-18
C-16	Construction of LCD Panel	C-19
C-17	Operation Theory of LCD Panel.....	C-20

List of Tables

TABLE NUMBER	DESCRIPTION	PAGE NUMBER
4-1	I/O MAP	4-5
4-2	Port Address of PIO	4-5
4-3	System Bus Pin Assignments	4-11
B-1	System Bus Connector Pin Assignments	B-2
B-2	RS-232C Connector Pin Assignments	B-3
B-3	Printer Connector Pin Assignments	B-4
C-1	Interrupt Priority, Restart Address and Sensitivity	C-4
C-2	80C85A Machine Cycle Chart	C-6
C-3	80C85A Machine State Chart	C-6
C-4	I/O Address of 81C55.....	C-9
C-5	Port Control Assignment.....	C-10
C-6	Control Word Format	C-15

I. INTRODUCTION

This manual is prepared for the Tandy 102 technicians working in field or in repair centers. Users of this manual should be acquainted with the 80C85A microprocessor, the 81C55 PIO and the 6402 UART. If you need more detailed information, refer to Appendix C in this manual.

This manual consists of seven sections and three appendices:

Section I

This section provides general information on the Tandy 102 such as specifications, external views and internal views.

Section II

This section describes the disassembly procedures.

Section III

This section describes the maintenance of the Tandy 102.

Section IV

This section describes the general theory of operation for the Tandy 102.

Section V

This section describes how to troubleshoot the Tandy 102.

Section VI

This section provides an exploded view and parts list of the Tandy 102.

Section VII

This section provides the schematics, PCB diagrams, and silkscreen views of the PCBs of the Tandy 102.

Appendix A

This appendix provides instructions for installing the optional ROM and additional RAMs.

Appendix B

This appendix provides the character code table, keyboard layouts and connector pin assignments.

Appendix C

This appendix provides the technical information of the 80C85A, 81C55, 6402 and LCD.

System Overview

Tandy 102 portable computer is a low cost version of the Radio Shack TRS-80 Model 100 Portable Computer. The Tandy 102 is fully compatible with the Model 100 in its software so that both system users can take advantage of the large number of programs available.

The Tandy 102 has the following applications programs in the standard ROM: BASIC, TEXT, TELCOM, ADDRSS, SCHEDL and TELCOM.

External View

- 1 Keyboard:** Can be used like the standard typewriter. However, the Tandy 102 does have a few special keys. (See Appendix B of this manual for more details.)
- 2 LCD Screen:** The Tandy 102 display has eight lines that allow 40 characters on each line.
- 3 Power Switch:** Move this switch towards the front to turn the power on. To conserve the batteries, the Tandy 102 automatically turns the power off if you do not use it for 10 minutes in default setting.
- 4 Low Battery Indicator:** Before the Tandy 102 is operational batteries become exhausted, this indicator will illuminate.
- 5 Display Adjustment Dial:** This control adjusts the contrast of the LCD display relative to the viewing angle.
- 6 External Power Adapter Connector:** Connect the appropriate and of Radio Shack's AC Power Supply (Catalog Number 26-3804, optional/extra) to this connector. Connect the other end of the power supply to a standard AC wall-outlet or approved power strip.

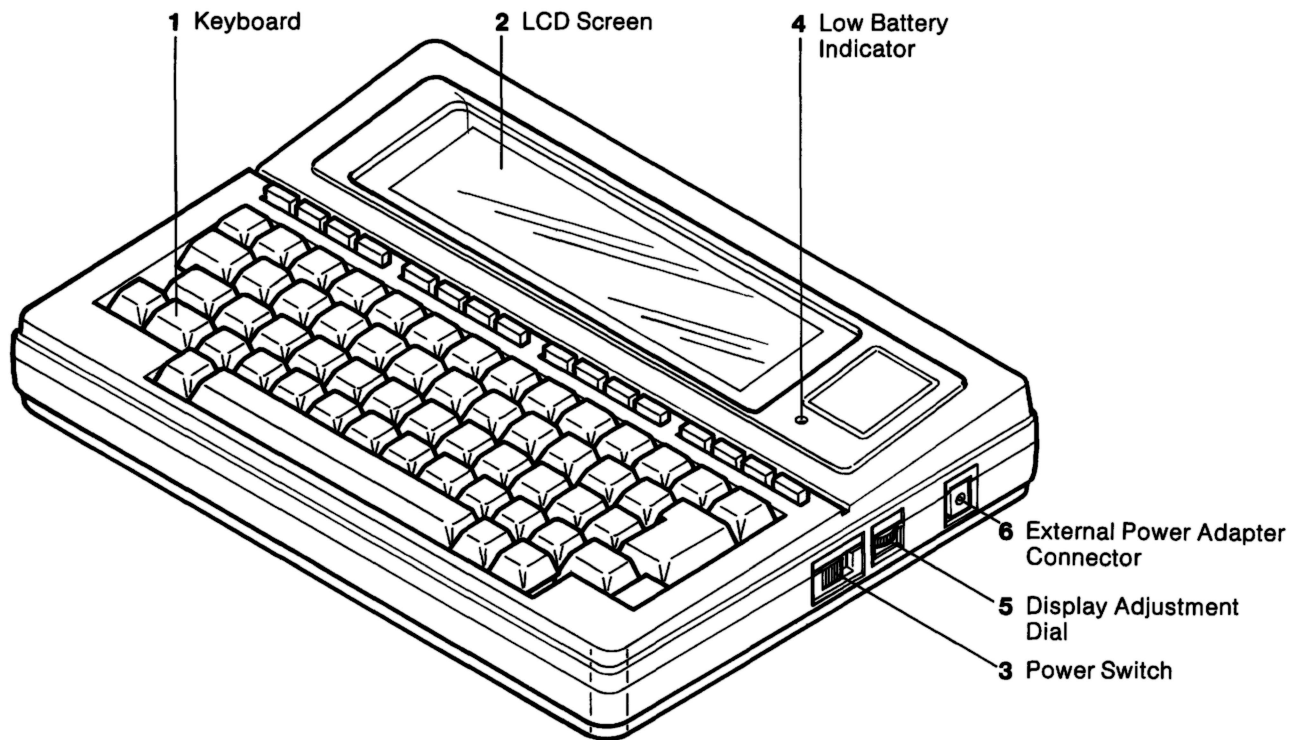


Figure 1-1. Front View

- 1 **RESET Switch:** If the Tandy 102 "locks up" (i.e., the display "freezes" and all keys seem to be inoperative), press this button to return to the Main Menu (start-up). It is not likely that the Tandy 102 will lock-up when you are using the built-in applications programs, however, it may occur with customized programs.
- 2 **RS-232C Connector:** Attach a DB-25 cable (such as Radio Shack Catalog Number *26-1408*) to this connector when you need to receive or transmit serial information. When you communicating directly with another TRS-80 computer, a Null MODEM Adapter (*26-1496*) is required. An 8" Cable Extender (*26-1497*) may also be required.
- 3 **SYSTEM BUS Connector:** Connect this connector to the TRS-80 Disk/Video interface (*26-3806*), using the system bus cable.
- 4 **PRINTER Connector:** For hard-copy printouts of information, attach any Radio Shack parallel printer to this connector, using an optional/extra printer cable.
- 5 **Direct-Connect MODEM (PHONE) Connector:** When communicating with another computer via the Tandy 102's built-in MODEM, connect the round end of the optional/extra MODEM cable to this connector.
- 6 **CASSETTE Recorder Connector:** To save or load information, on a cassette tape, connect the cassette recorder here. An optional/extra cassette recorder (and cable) is required.
- 7 **Bar Code Wand Connector:** Attach the optional/extra bar code wand to this connector. Note that special bar code reader software is required.
- 8 **DIR/ACP Selector:** This selector allows you to select either a direct or acoustic coupler connection. If you are communicating with another computer over the phone lines via the built-in, direct-connect MODEM, set this switch to the DIR position. If you are using the optional/extra Model 100 Acoustic Coupler (*26-3805*), set this connector to the ACP position.
- 9 **ANS/ORIG Selector:** If you are "originating" a phone call to another computer, set this switch to ORIG. If another computer is calling your Tandy 102, set to ANS.

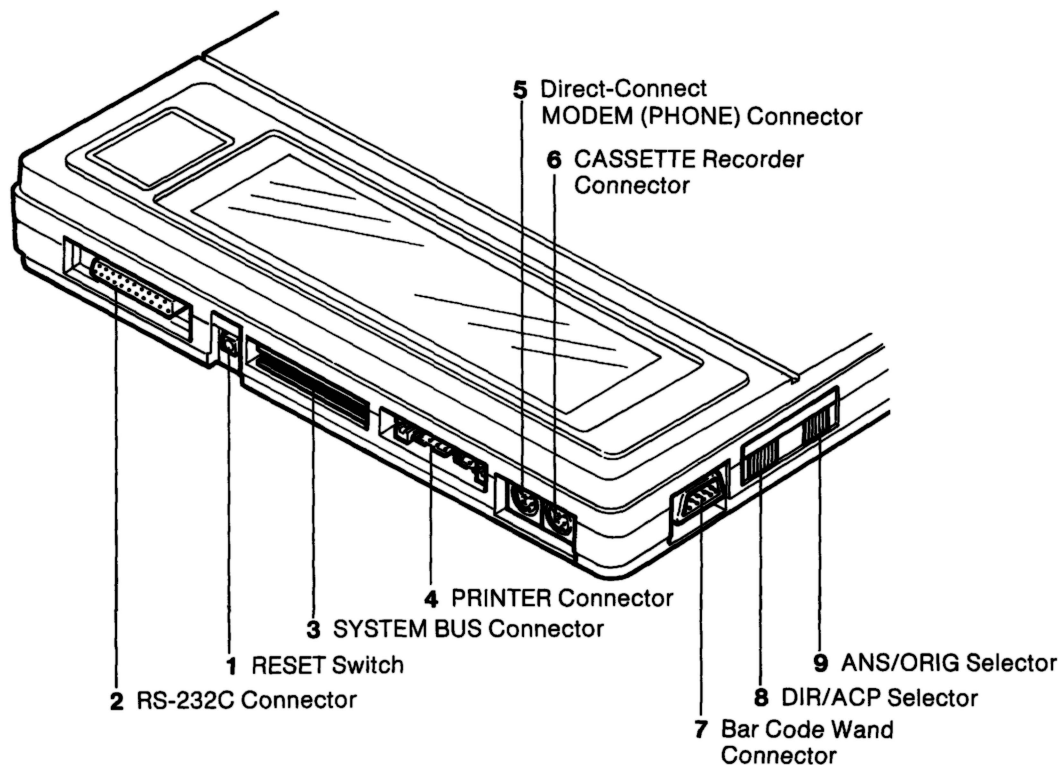


Figure 1-2. Rear View

- 1 MEMORY POWER Switch:** This switch is used to prevent discharge of the internal Nickel-Cadmium battery, which is used for RAM back-up. The Tandy 102 will operate only when the power switch is set to ON. Set this switch to the OFF position when the Tandy 102 will not be used for a long period of time. Note that the RAM will not be backed up when this switch is set to the OFF position.
- 2 Optional ROM and RAM Compartment:** An optional/extra ROM and RAM can be inserted into this compartment to enhance the Tandy 102 capabilities.
- 3 Battery Compartment:** When not connected to an AC power source, the Tandy 102 gets its power from four AA size batteries that must be installed in this compartment.

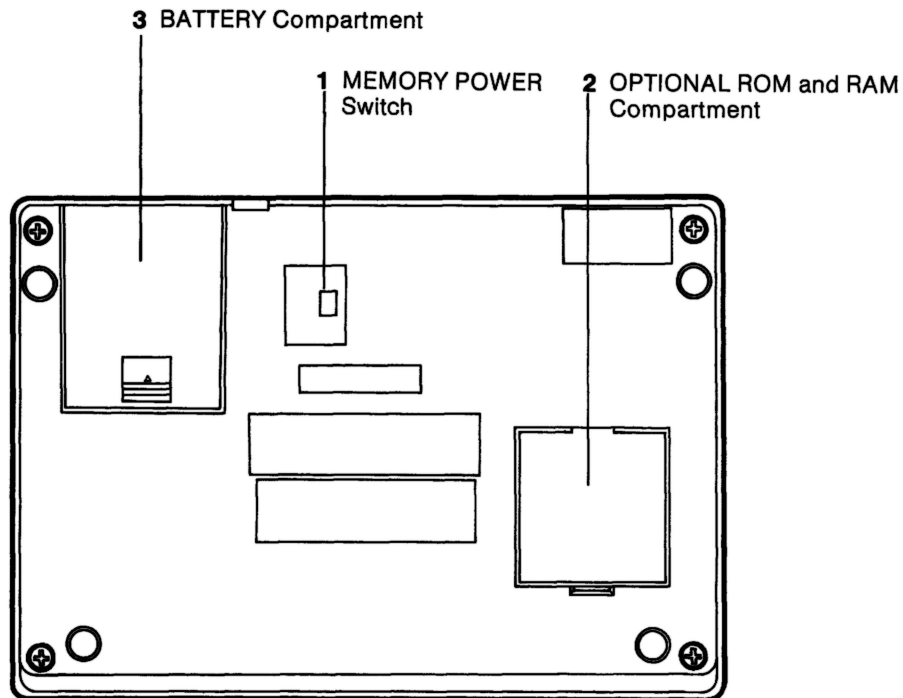


Figure 1-3. Bottom View

Internal View

The Tandy 102 consists of three printed circuit boards:

- LCD PCB
- Keyboard PCB
- Main PCB

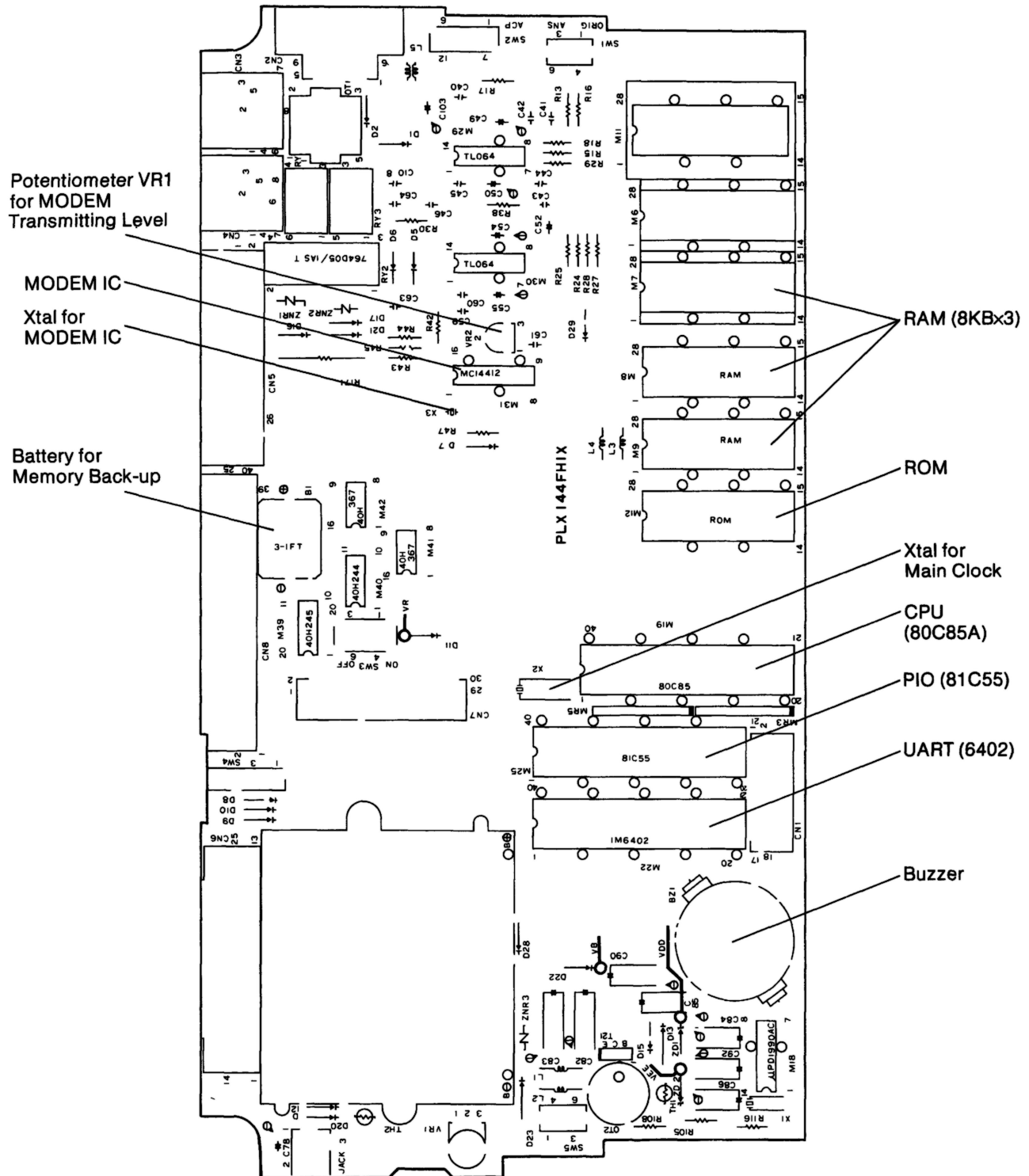


Figure 1-4. Main PCB (Bottom View)

Specifications

Main Components

Keyboard

Life of key switch	
Number of keys	72 keys (8 × 9 key matrix)
Function keys	3 millions keystrokes
Caps/NUM lock key	0.5 million keystrokes
Other keys	5 millions keystrokes

LCD display

Display panel	240 × 64 full-dot matrix 1/32 duty 1/6.66 bias
Dot pitch	0.8 × 0.8 mm
Dot size	0.73 × 0.73 mm
Effective display area	191.2(W) X 50.4(D) mm

Operation batteries

Batteries	Four type AA Alkaline-manganese batteries
Operation time	5 days (Typ.) — 4 hours per day 20 days (Typ.) — 1 hour per day (Note: without I/O units at normal temperature)

Memory protection battery (On Main PCB)

Battery	Rechargeable battery (50mAh/3.6V)
Back-up time	More than 20 days-16 KB RAM More than 10 days-32 KB RAM
Recharge method	Trickle charge by AC adapter operation batteries
Charging current	1.2 mA (Typ.)

LSIs

CPU	80C85A Code and pin compatible with 8085
ROM	Maximum 64 KB Standard 32 KB Optional 32 KB
RAM	Maximum 32 KB Standard 24 KB Optional 8 KB

Power consumption

65 mA (Typ.)

Dimensions

11-3/4" (W) X 8-1/2" (D) X 1-1/2" (H)
300 (W) X 215 (D) X 38.5 (H) mm

Weight

3 lbs. 2 oz. (with batteries)
1.4 kg

I/O Interface

RS-232C

Conforms to EIA standard signal

TXR (Transmit Data)
RXR (Receive Data)
RTS (Request to Send)
CTS (Clear to Send)
DSR (Data Set Ready)
DTR (Data Terminal Ready)

Communications protocol

Word length

6, 7, or 8 bits

Parity

NONE, EVEN or ODD

Stop bit length

1 or 2 bits

Baud rate

75, 110, 300, 600, 1200, 2400,
4800, 9600 or 19200 BPS

Maximum transmission distance

5 meters

Maximum driver output voltage

± 5 volts

Minimum driver output voltage

± 3.5 volts

Maximum receiver input voltage

± 18 volts

Minimum receiver input voltage

± 3 volts

MODEM/Coupler

Conforms to BELL 103 Standard

Data length

6, 7 or 8 bits

Parity

NONE, EVEN or ODD

Stop bit length

1 or 2 bits

Baud rate

300 BPS

Full duplex

Answer mode/originate mode switchable

Transmit output level

15 dBm \pm 2dBm

Receive sensitivity

-30 dBm

Other functions

Hang-up function

Auto pulse dialing function

10/20 PPS

Printer interface

Conforms to Centronics interface standards

Handshake signals

$\overline{\text{STROBE}}$, $\overline{\text{BUSY}}$, $\overline{\text{BUSY}}$

Audio cassette interface

Data rate

1500 BPS

(Mark 2400 Hz, Space 1200 Hz)

Input level

0.8 to 5 volts (Peak to peak)

Output level

580 mV \pm 10%

Bar code reader interface

Input level

3.5 volts (Min.)-High

1.5 volts (Max.)-low

II. DISASSEMBLY INSTRUCTIONS

Cases

1. Disconnect the cables from the unit.
Taking care not to scratch the LCD screen and key tops, turn the unit over and remove 4 screws A from the upper and lower cases.
2. Remove the upper case.
Therefore, the upper and lower cases are secured by snaps. Pull up the front of the upper case first, as shown below.
Also, do not apply too much force when pulling it.

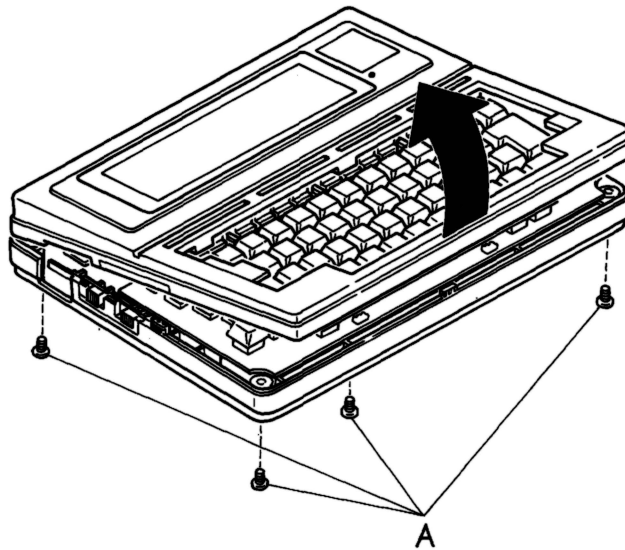


Figure 2-1. Top Case Removal

Keyboard and LCD PCBs

1. Disconnect the flat cable from the connector on the keyboard PCB.
2. Remove the keyboard PCB.
3. Disconnect the flat cable from the connector on the LCD PCB.
4. Remove the LCD PCB.

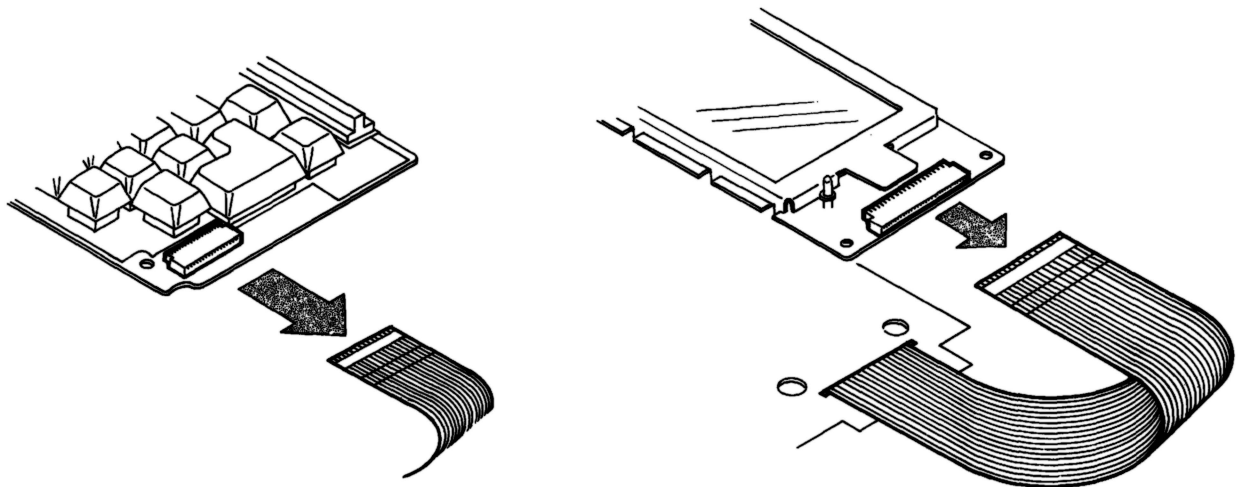


Figure 2-2. Keyboard and LCD PCBs Removal

Main PCB

1. Remove the insulator board.
2. Remove 2 screws B securing the main PCB and bottom case.
3. Remove the main PCB.

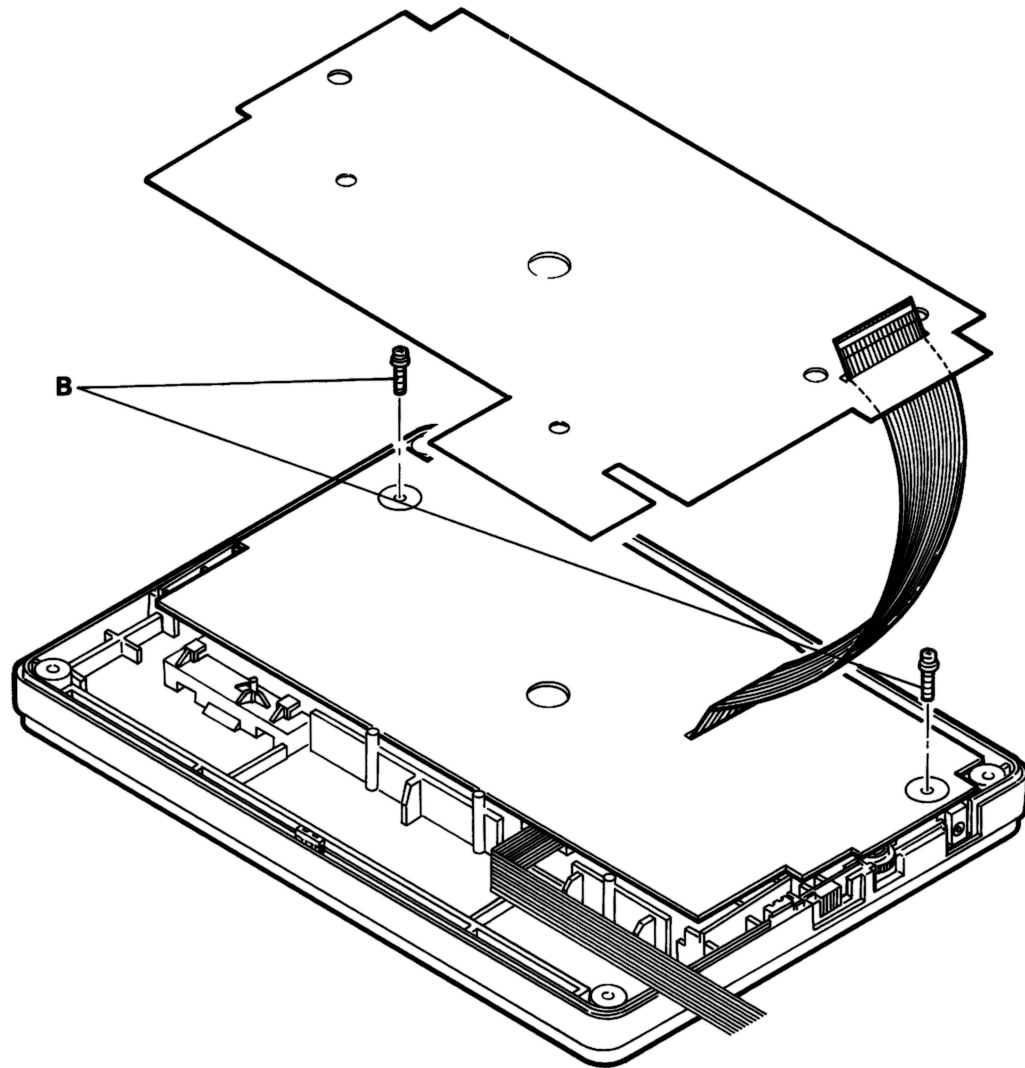


Figure 2-3. Main PCB Removal

III. MAINTENANCE

To Clean the Body and LCD Display

1. To avoid operational trouble, always keep the Tandy 102 clean.
2. Clean the body and the LCD screen using a soft, dry, lint-free cloth.
3. For tough stains, clean the body or the LCD screen with benzol.

Caution: Do not use any solvents other than benzol.

IV. THEORY OF OPERATION

General

Figure 4-1 shows how this section is organized and highlights significant areas.

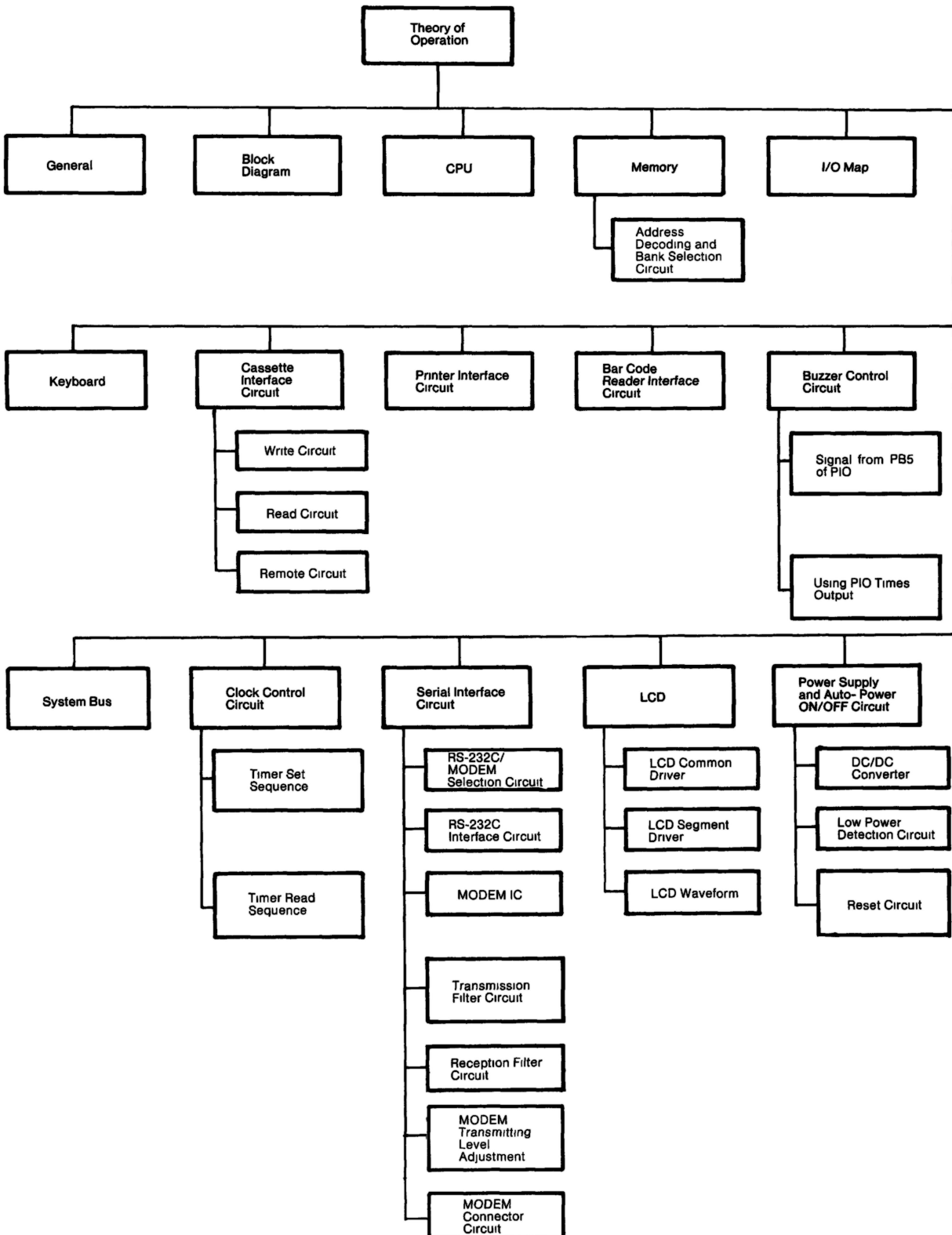


Figure 4-1. Organization of Section IV

Block Diagram

The Tandy 102 has three principal LSIs.

- **80C85A CPU**

This is the Central Processing Unit which controls all functions.

- **81C55 PIO**

This is the Parallel Input/Output interface controller which controls the printer interface, keyboard, buzzer, clock and LCD interface.

- **6402 UART**

This is the Universal Asynchronous Receiver Transmitter which controls the serial interface (RS-232C or MODEM).

The input/output for a cassette recorder and the input of the BCR are controlled by CPU directly through its SOD, SID and RST5.5 terminals.

ROM and RAMs are connected to the system bus. ROM is available only for alternative selection from Standard or Option.

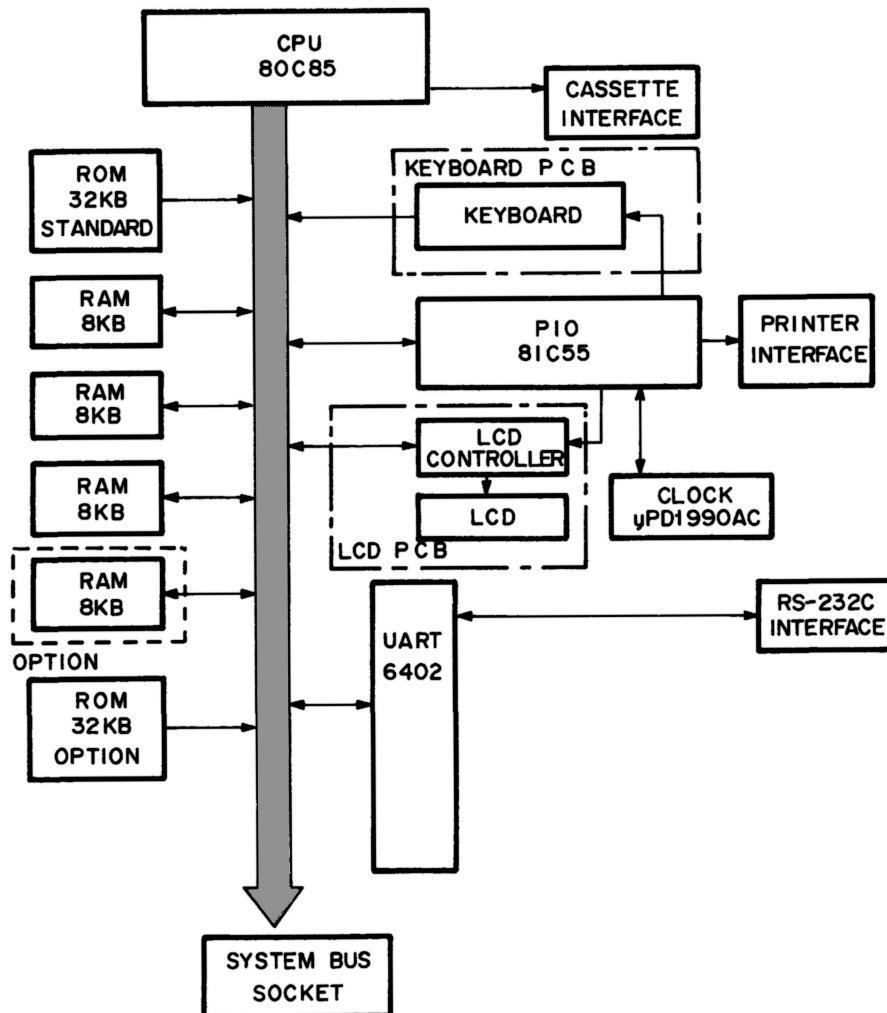


Figure 4-2. System Block Diagram

CPU

The CPU is an 80C85A that runs at a clock speed of 2.4576 MHz. It is an 8-bit, parallel Central Processing Unit using C-MOS technology. The instruction set is fully compatible with the 8085A microprocessor. The 80C85A uses a multiplexed data bus. The CPU bus is divided into two sections—the 8-bit address bus named the A8-A15, and the 8-bit address and data bus named the AD0-AD7. The address bus signals are separated at M1, using the ALE* (Address Latch Enable) signal.

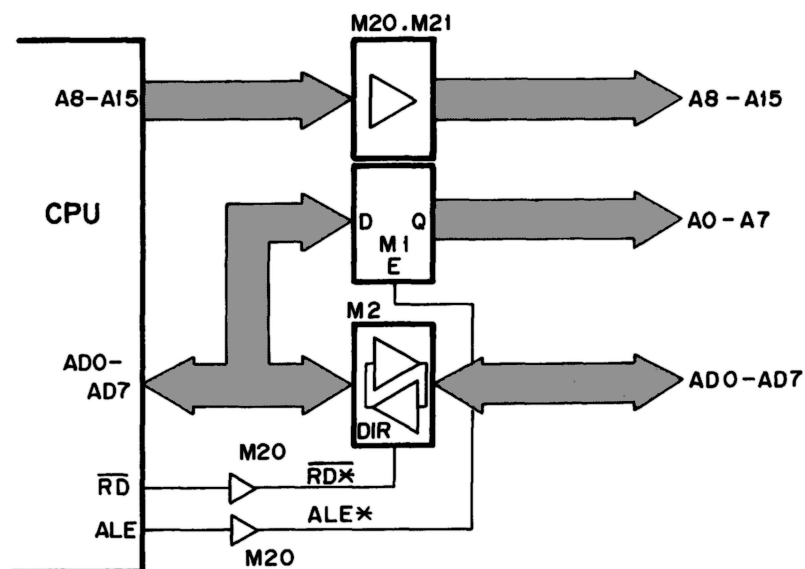


Figure 4-3. Functional Block Diagram of Bus Separation Circuit

Memory

The memory of the Tandy 102 consists of a 32 KB standard ROM, three 8 KB C-MOS static RAMs and a 32 KB optional ROM.

The standard RAMs equipped in the Tandy 102 are M9, M8 and M7. By installing M6, memory capacity can be increased to 32 KB. The ROM used in the Tandy 102 is a 32 KB (256K bits) memory.

It is operated only by a +5V power source with an access time of 600 nsec (Max.).

The BASIC program and BIOS program which operate the LCD, printer etc. are stored in the standard ROM.

An optional ROM can be installed onto the special IC socket by removing the ROM cover on the bottom case of the Tandy 102. Various types of application programs are stored in the optional ROM.

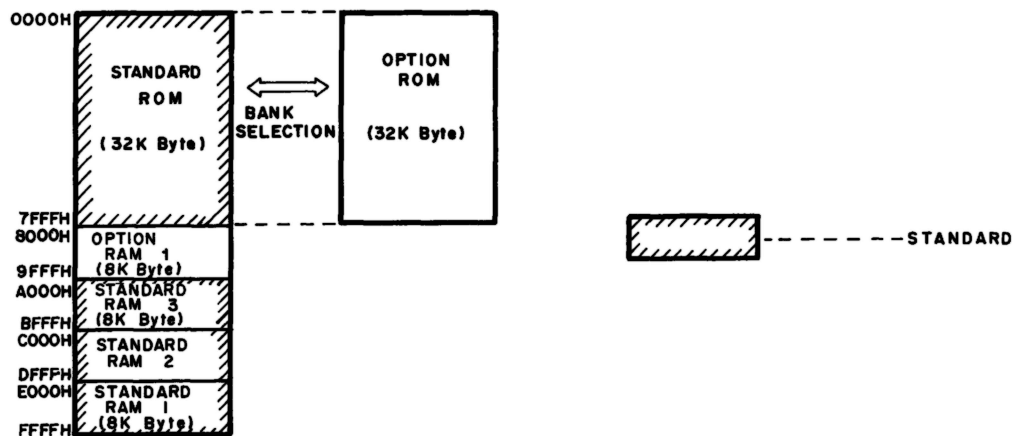


Figure 4-4. Memory Map

Address Decoding and Bank Selection Circuit

Although four 8 KB static RAMs and two masked ROMs can be installed in the Tandy 102, six chip-select signals are required.

Because the RAMs are positioned from 8000H to FFFFH, and ROMs are positioned from 0000H to 7FFFH, address signal A15 selects the ROMs or RAMs at M5. At another section of M15, address signals A14 and A13 select each RAM corresponding to the memory map. The ROMs (both standard and optional) installed in the Tandy 102 are the 32 KB 1-chip type. As shown in the memory map, the address space is positioned from 0000H to 7FFFH.

The chip select signals are generated by the A15 and \overline{STROM} signals. The AD0 is latched at M14 by the \overline{WR} signal and $\overline{Y6}$ signal, and then the \overline{STROM} signal is generated.

The standard ROM is selected by the low level \overline{STROM} signal and the optional ROM is selected by the high level \overline{STROM} signal.

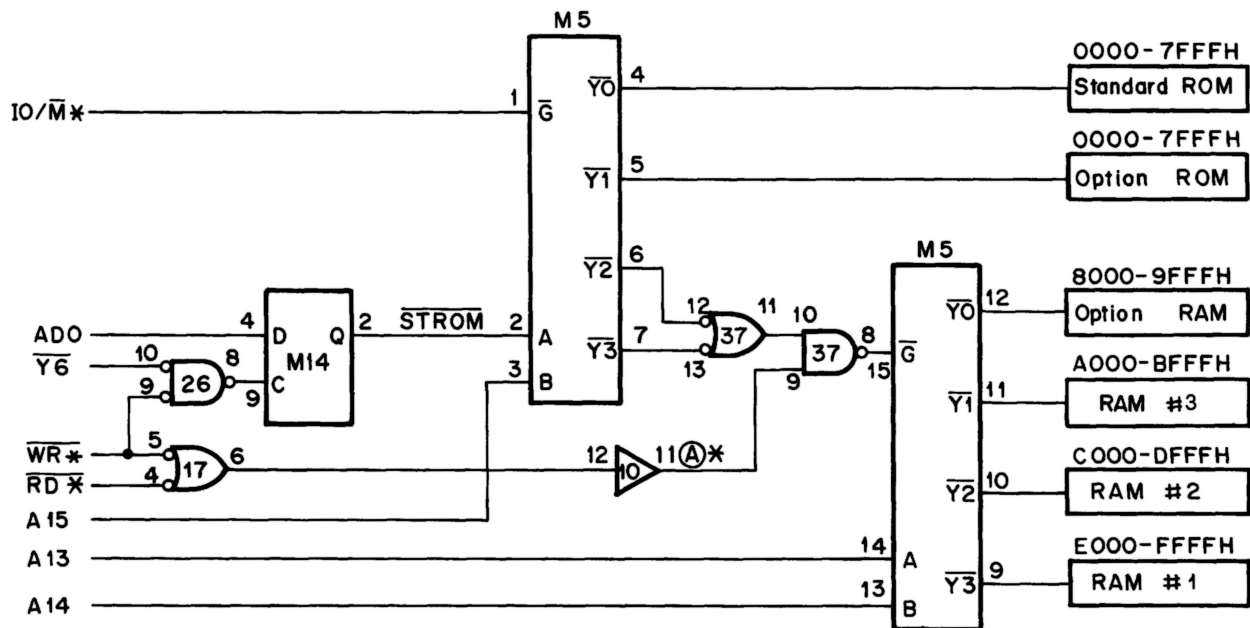


Figure 4-5. Address Decoding and Bank Selection Circuit

I/O MAP

As shown in the figure below, the I/O address decoding circuit, consisting of M16, decodes address signals A12 to A15 and generates I/O selection signals $\overline{Y0}$ to $\overline{Y7}$.

The application of the selection signals ($\overline{Y0}$ to $\overline{Y7}$) for the I/O devices are shown in Table 4-1.

Table 4-2 shows the port address of the PIO.

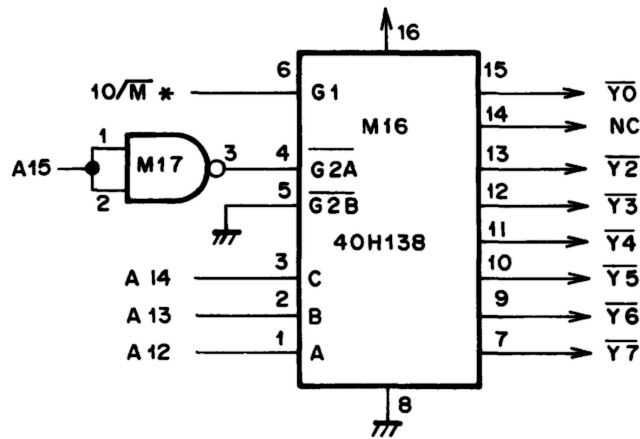


Figure 4-6. I/O Address Decoding Circuit

Address	Signal	Active Level	Application
00H – 7FH	—	—	Free area for an optional unit and other select signals of various circuits made by user.
80 – 8FH	$\overline{Y0}$	L	Device-select signal for optional I/O controller unit.
90H – 9FH	$\overline{Y2}$	L	Enable signal for relay RY3 in MODEM connector interface circuit.
B0H – BFH	$\overline{Y3}$	L	PIO (81C55) chip-select signal.
C0H – CFH	$\overline{Y4}$	L	Enable signal for data input/output port of UART.
D0H – DFH	$\overline{Y5}$	L	Enable signal to set various modes and read port of UART.
E0H – EFH	$\overline{Y6}$	L	Enable signal for \overline{STROM} and REMOTE, and input data from keyboard. Strobe signal for printer and clock.
F0H – FFH	$\overline{Y7}$	L	Enable signal for LCD driver LSI.

Table 4-1. I/O Map

Address	Port or Register
B0H or B8H	Command/status register (internal)
B1H or B9H	Port A
B2H or BAH	Port B
B3H or BBH	Port C
B4H or BCH	Timer register lower byte
B5H or BDH	Timer register upper byte
B6H, B7H, B8H and B9H	Not used

Table 4-2. Port Address of PIO

Keyboard

Key strobe signals are emitted from the PA0 to PA7 and PB0 terminals of the PIO. The return signals from the keyboard pass through the bus buffers (M15 and M3) and send to the CPU. The I/O address of the return signals is E0H-EFH.

The condition of pressing the “T” key is shown in the figure below.

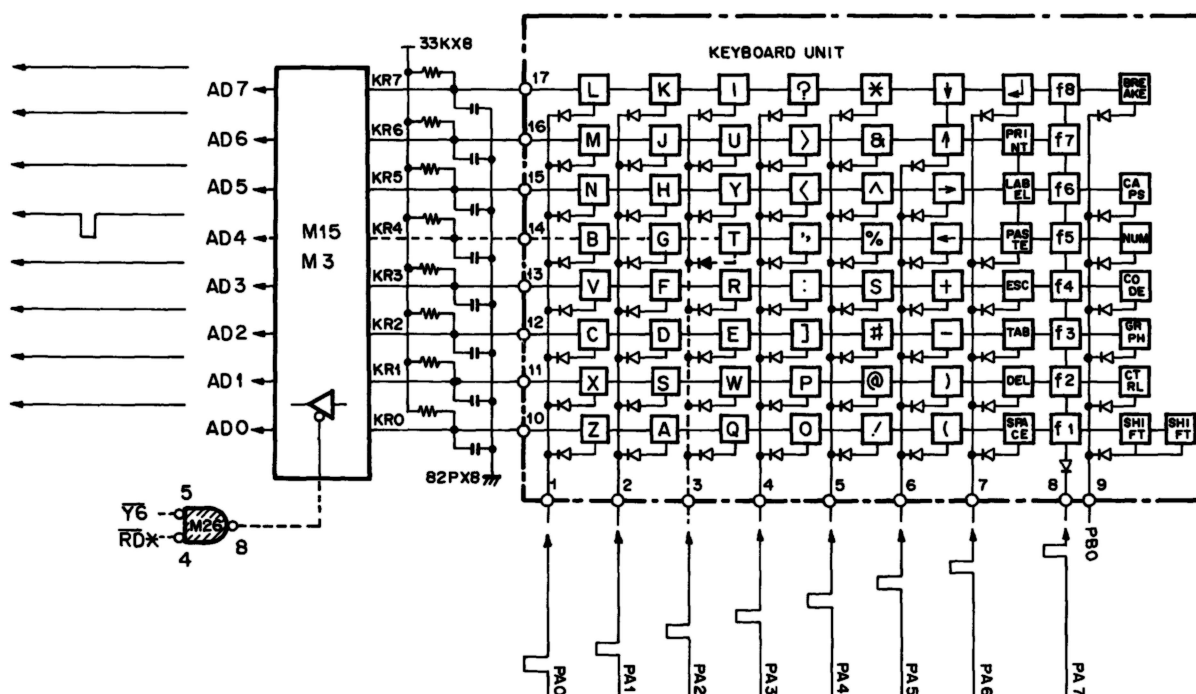


Figure 4-7. Condition of Pressing “T” Key

Cassette Interface Circuit

The cassette interface circuit is subdivided into three sections:

- Write circuit
- Read circuit
- Remote circuit

Write Circuit

The write circuit is accomplished in several steps. First, the serial data from the SOD terminal of the CPU is inverted by M34. Then, the DC component is removed by C63. Finally, the data passes through an integrator consisting of R51 and C64, and after voltage division, out to a cassette recorder AUX jack.

Read Circuit

The signal input from the earphone jack of the cassette recorder passes through the clamp circuit consisting of D5 and D6, and then is input to the comparator circuit consisting of M30. Finally, the signal is converted into the digital signal and sent to the SID terminal of the CPU. In this circuit, D7 clamps the negative voltage output of the comparator.

Remote Circuit

As a result of writing data "1" into bit 3 of the output port (M14) specified by I/O address E0H-EFH, the REMOTE signal is changed to H level.

Then, T6 is switched on and relay RY1 is energized. This causes the drive motor of the cassette recorder to operate.

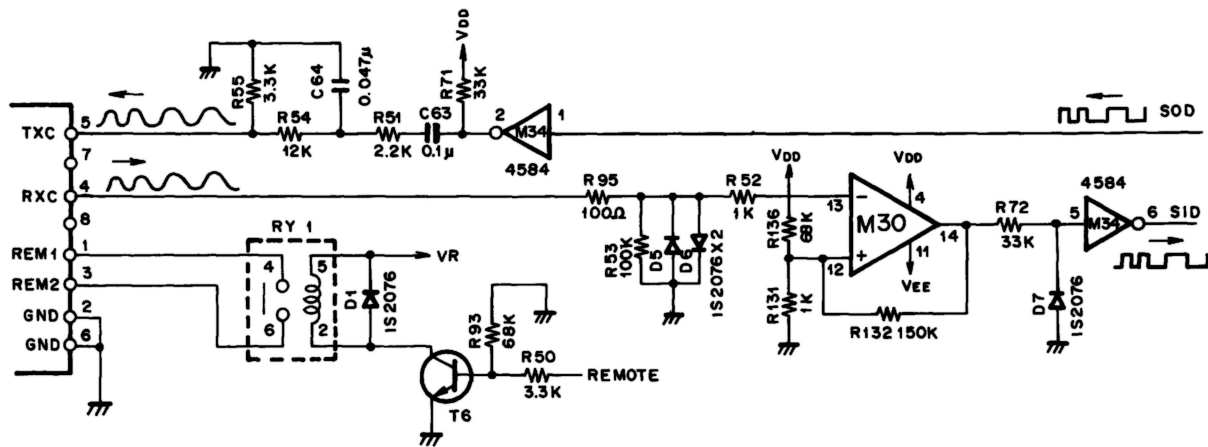


Figure 4-8. Cassette Interface Circuit

Printer Interface Circuit

The printer interface circuit conforms to Centronics standards. As shown in Figure 4-9, the BUSY signal from the printer is read from the PC2 of the PIO. If the condition is not busy (PC2 = L), the 8-bit parallel data (PA0 – PA7) is sent to the printer. Then, by writing data "1" into bit 1 of the output port specified by I/O address E0H-EFH, the $\overline{\text{PSTB}}$ signal is sent to the printer.

As soon as the printer receives this $\overline{\text{PSTB}}$ signal, the BUSY signal is changed to H indicating that the printer is busy. The CPU then waits for a while until this BUSY signal becomes L. The printer prints the one character corresponding with the 8-bit parallel data. After completion of the one character printing, the printer sets the BUSY signal to L. Then, the CPU sends the next 8-bit parallel data. If the printer is in ONLINE condition, the $\overline{\text{BUSY}}$ signal is H and sent to the CPU, passing through the PC1 of the PIO. However, when in the OFFLINE condition, the $\overline{\text{BUSY}}$ signal is L and transmission of print data to the printer is inhibited by the CPU.

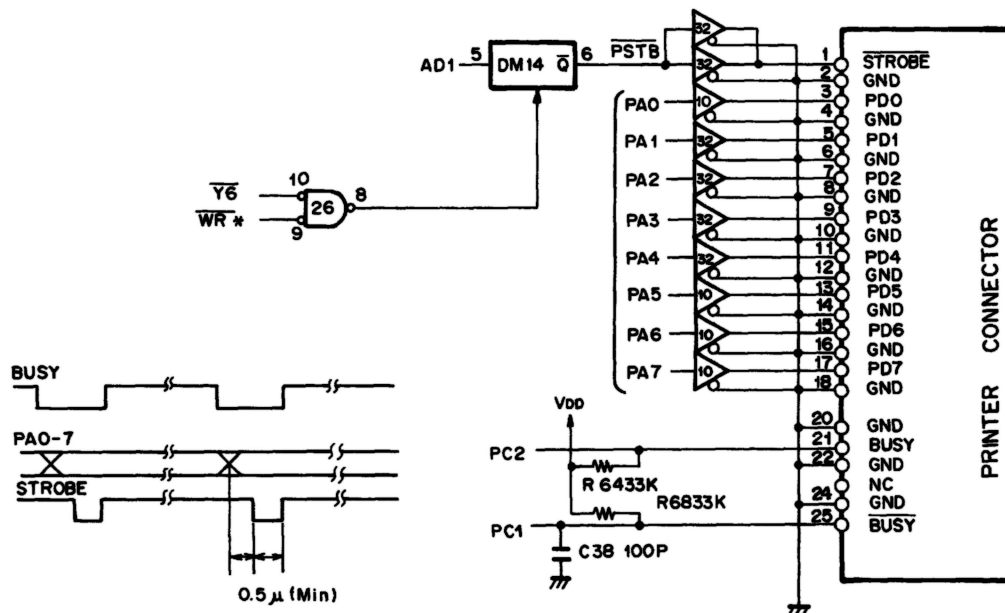


Figure 4-9. Printer Interface Circuit

Bar Code Reader Interface Circuit

The input signal from the bar code reader is subjected to waveform shaping, inverted by the Schmitt-type inverter (M34), and then sent to the PC3 terminal of the PIO and the RST5.5 terminal of the CPU.

When the bar code reader reads the first white part of the bar code, a L level signal is generated, then inverted by M34 to notify the CPU of an interruption. As soon as RST5.5 interruption occurs, the CPU starts the data input operation, passing through the PC3 of the PIO. As the bar code reader is moved across the bars, H and L signals (which correspond to the white and black bars, respectively) are generated continuously and inversion signals are sent to the PC3 of the PIO as the serial input data stream.

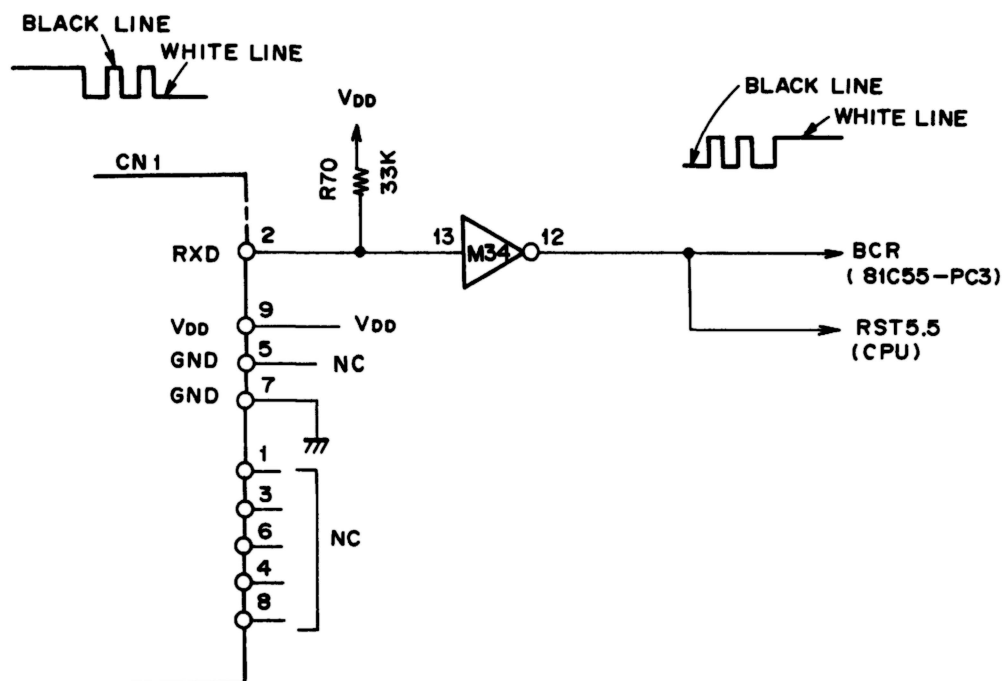


Figure 4-10. Bar Code Reader Interface Circuit

Buzzer Control Circuit

There are two ways to operate the buzzer. One is to sound the buzzer with the specified frequency by emitting signals from the PB5 of the PIO and the other, by using the timer output signal of the PIO.

Signal from PB5 of PIO

When the PB2 of the PIO is H, the buzzer sounds by repeated switching of the buzzer driving transistor. This is caused by H, L, H, L ... output signals from the PB5 synchronizing with the frequency for sounding the buzzer. This method is used for the BEEP command in BASIC.

PIO Timer Output

In this method, the buzzer is sounded by setting the PIO timer in the square wave output mode. To write the value corresponding to the sound frequency, the CPU assigns B4H, B5H, BCH or BDH to the I/O port address. This frequency is assigned by the first parameter of the SOUND command in BASIC.

If the above procedures are completed, the TO terminal of the PIO outputs the square waves, and the PB2 of the PIO controls the length of the sound whenever the PB5 is "L". How long the sound is heard depends on the second parameter of SOUND command in BASIC.

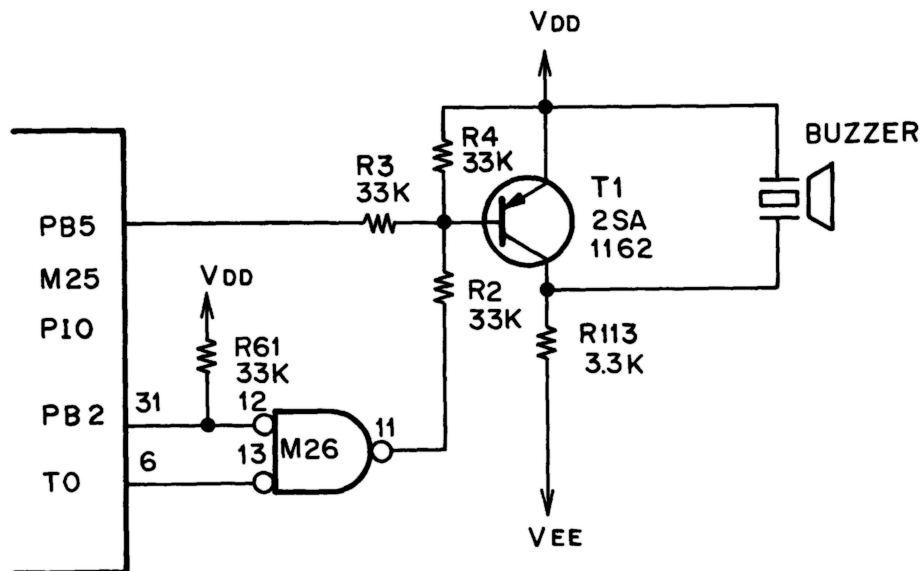


Figure 4-11. Buzzer Control Circuit

System Bus

In order to expand the use of external devices, a 40-pin system bus connector is mounted on the back panel of the Tandy 102.

As shown in the Table 4-3, the address bus, data bus and control bus can be connected to the external devices passing through the drivers or receivers, thus making system expansion easy.

Pin No.	Signal	Description
1	VDD	+5V power supply
2	VDD	+5V power supply
3	GND	Ground
4	GND	Ground
5	AD0	Address and data signal bit 0
6	AD1	Address and data signal bit 1
7	AD2	Address and data signal bit 2
8	AD3	Address and data signal bit 3
9	AD4	Address and data signal bit 4
10	AD5	Address and data signal bit 5
11	AD6	Address and data signal bit 6
12	AD7	Address and data signal bit 7
13	A8	Address signal bit 8
14	A9	Address signal bit 9
15	A10	Address signal bit 10
16	A11	Address signal bit 11
17	A12	Address signal bit 12
18	A13	Address signal bit 13
19	A14	Address signal bit 14
20	A15	Address signal bit 15
21	GND	Ground
22	GND	Ground
23	RD*	Read enable signal
24	WR*	Write enable signal
25	IO/M*	I/O or memory select signal
26	S0	Status 0 signal
27	ALE*	Address latch enable signal
28	S1	Status 1 signal
29	CLK	Clock signal
30	Y0	I/O controller select signal
31	A*	I/O or memory access enable signal
32	RESET*	Reset signal
33	INTR	Interrupt request signal
34	INTA	Interrupt acknowledge signal
35	GND	Ground
36	GND	Ground
37	RAM RST	RAM enable signal
38	NC	No connection
39	NC	No connection
40	NC	No connection

Table 4-3. System Bus Pin Assignments

Clock Control Circuit

A clock LSI (μ PD1990AC) is used in the clock control circuit so that the time and date information can be set and read by the CPU.

As shown in Figures 4-12 to 4-13, when the Tandy 102 is in the operable condition ($\overline{\text{RESET}}$ is H), commands and data can be input and output to μ PD1990AC from the CPU at will. In addition, because back-up power supply VB is applied to the μ PD1990AC, the clock functions even when the Tandy 102 power switch is OFF.

The DATA IN, CLOCK and C0-C2 terminals of μ PD1990AC are connected to the PA0-PA4 terminals of the PIO. The DATA OUT terminal is connected to the PC0 terminal of the PIO. The STB signal is provided from bit 2 of the output port made by M14.

The TP terminal of the μ PD1990AC is connected to the RST7.5 terminal of the CPU. Square waves are output from the TP (4 ms cycle), and one key scan occurs every 4 ms because of the RST7.5 interruption to the CPU.

Time Set Sequence

The CPU set μ PD1990AC to the register shift mode with the "100" pattern of the C0-C2 and the strobe signal which is generated by the AD2, Y6 and $\overline{\text{WR}}^*$ signals passing through M14.

Then, the CPU sends the data of time and date information to the DATA IN terminal of μ PD1990AC with timing clock PA3.

Finally, the CPU sets μ PD1990AC to the time set mode with the "010" pattern of the C0-C2 and the strobe signal.

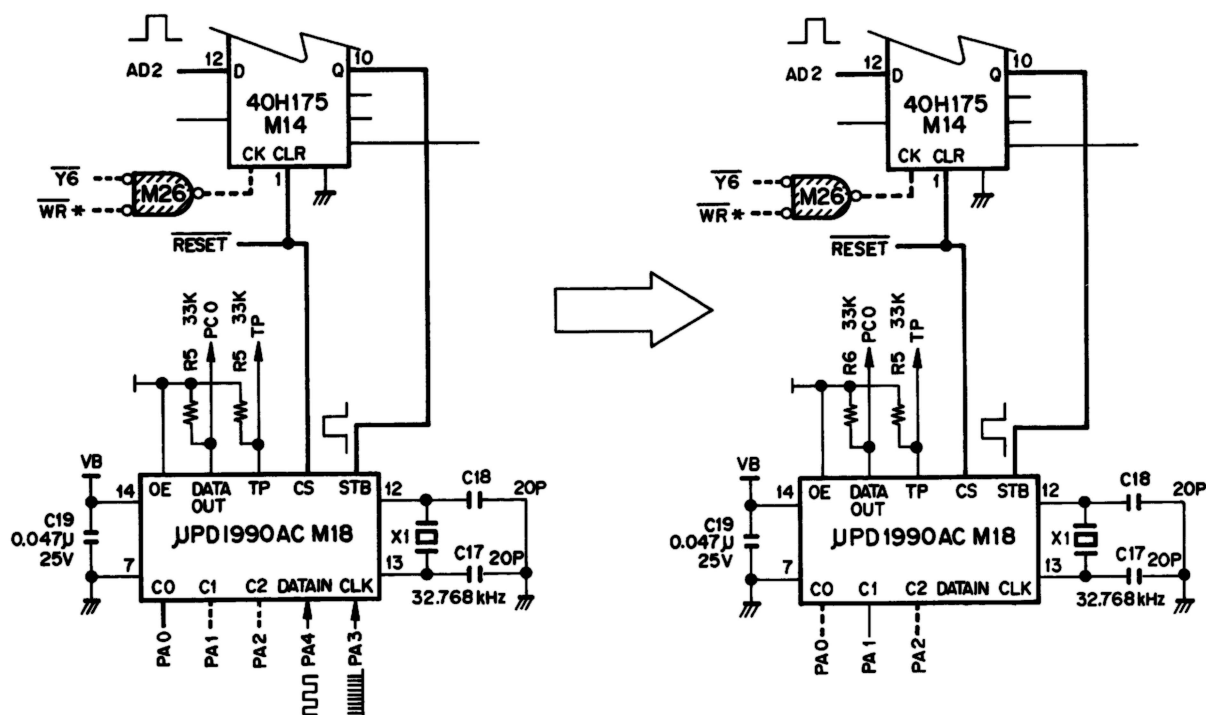


Figure 4-12. Time Set Sequence of μ PD1990AC

Time Read Sequence

The CPU sets the μ PD1990AC to the time read mode with the "110" pattern of the C0-C2 and strobe signal.

Then the CPU sets the register shift mode with the "100" pattern of the C0-C2, and reads the data of time and date information from the DATA OUT terminal. At the same time, the CPU sends the PA3 signal passing through the PIO for the read timing clock.

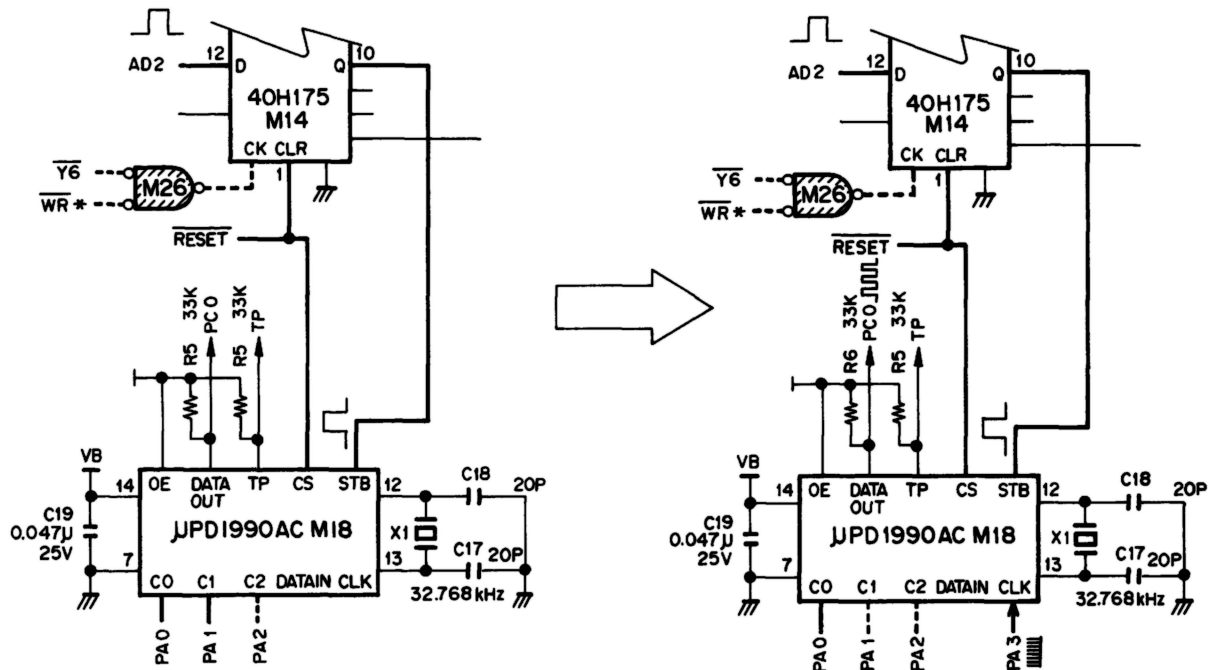


Figure 4-13. Time Read Sequence of μ PD1990AC

Serial Interface Circuit

The serial interface circuit supports asynchronous data transmission/reception. The heart of this circuit is the 6402 (UART). It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop and parity bits.

For a more detailed description of how this IC performs these functions, refer to Appendix C of this manual.

Figure 4-14 shows the functional block diagram of the serial interface circuit. In this figure, the TO signal, basic timing clock for the UART, defines the transmission/reception baud rate.

To transmit and receive the serial data from external devices, the RS232C signal selects either MODEM or RS-232C interface. During the MODEM operation, the MODE signal switches either the originate mode or answer mode for the MODEM IC.

The serial interface circuit is subdivided into the following circuits:

- RS-232C/MODEM Selection Circuit
- RS-232C Interface Circuit
- MODEM IC
- Transmission Filter Circuit
- Reception Filter Circuit
- MODEM Connector Circuit

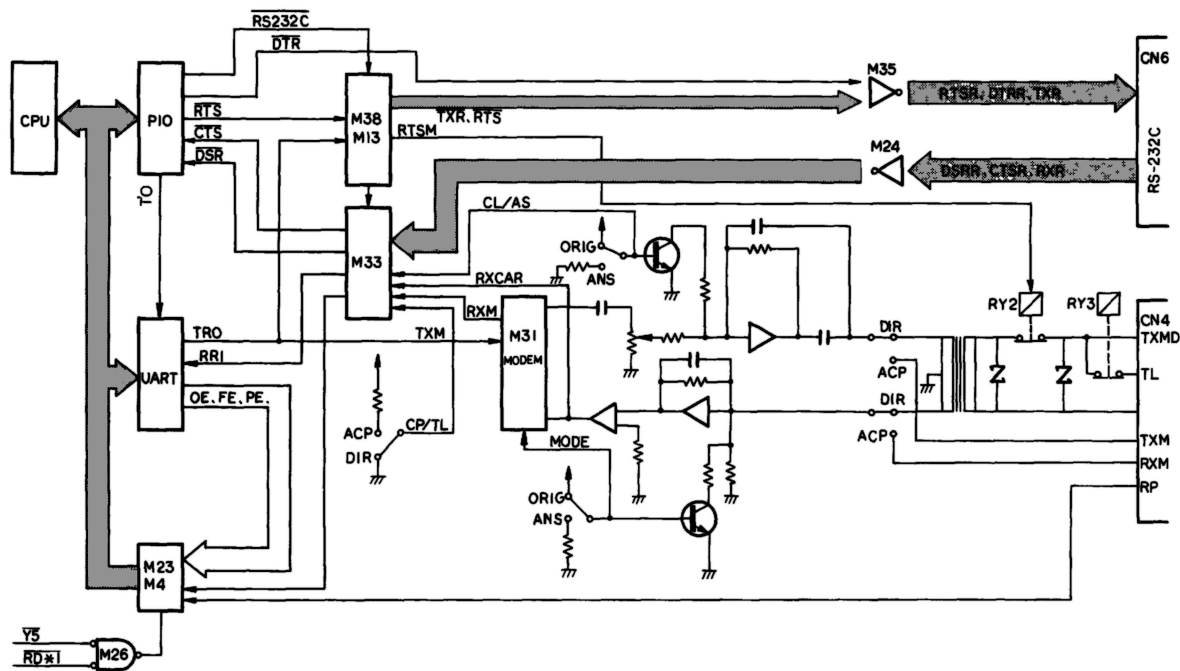


Figure 4-14. Functional Block Diagram of the Serial Interface

RS-232C/MODEM Selection Circuit

The RS232C signal (PB3 terminal of the PIO) determines whether the serial port is to be used for RS-232C or for MODEM. When the RS232C signal is H, the serial port is used for MODEM. The reception signals, including the control signals, are demultiplexed at M33.

During the RS-232C mode, the CD (Carrier Detect) signal is not used. To make this condition, pin 14 of M33 is connected to the ground.

During the MODEM mode, the CL/AS signal is used as the sensing signal for the ORG/ANS switch, and CP/TL signal is used as the sensing signal for the ACP/DIR switch. In order to detect the carrier signal from the telephone line, the CD signal is connected to the RXCAR terminal of the MODEM IC.

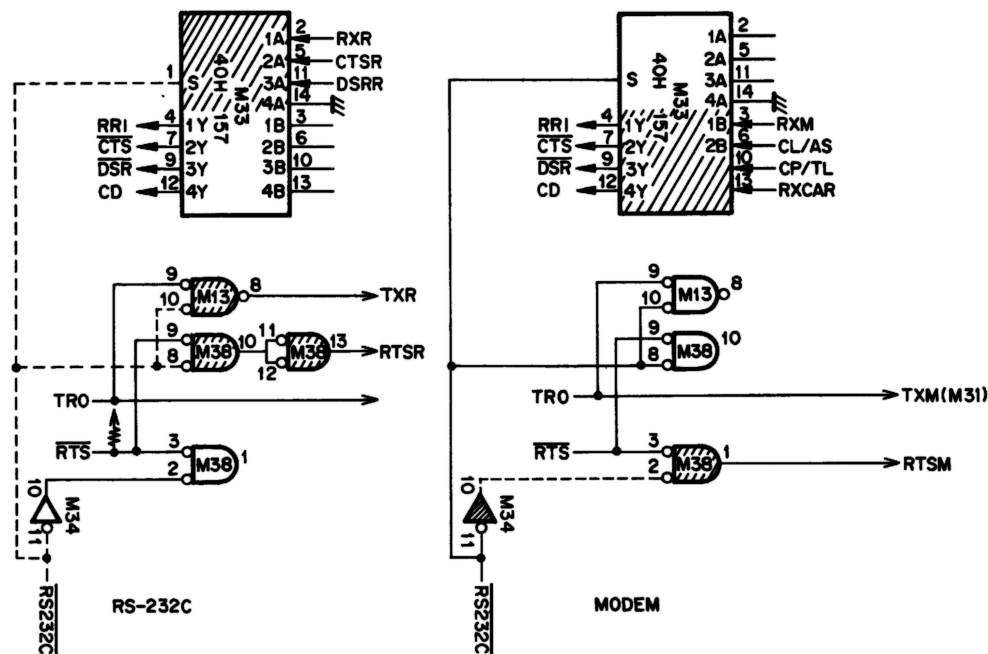


Figure 4-15. RS-232C/MODEM Selection Circuit

RS-232C Interface Circuit

In the RS-232C transmission circuit, after the DC component is removed from the signals by the coupling capacitors, the signals are leveled to $\pm 5V$ signals by the inverters connected in parallel, and then are output as RS-232C transmission signals.

In the RS-232C reception circuit, the DSRR, CTSR, and RXR signals from the external RS-232C line are subjected to waveform shaping and inverted by M24, and then converted to +5V or ground level signals by the diodes.

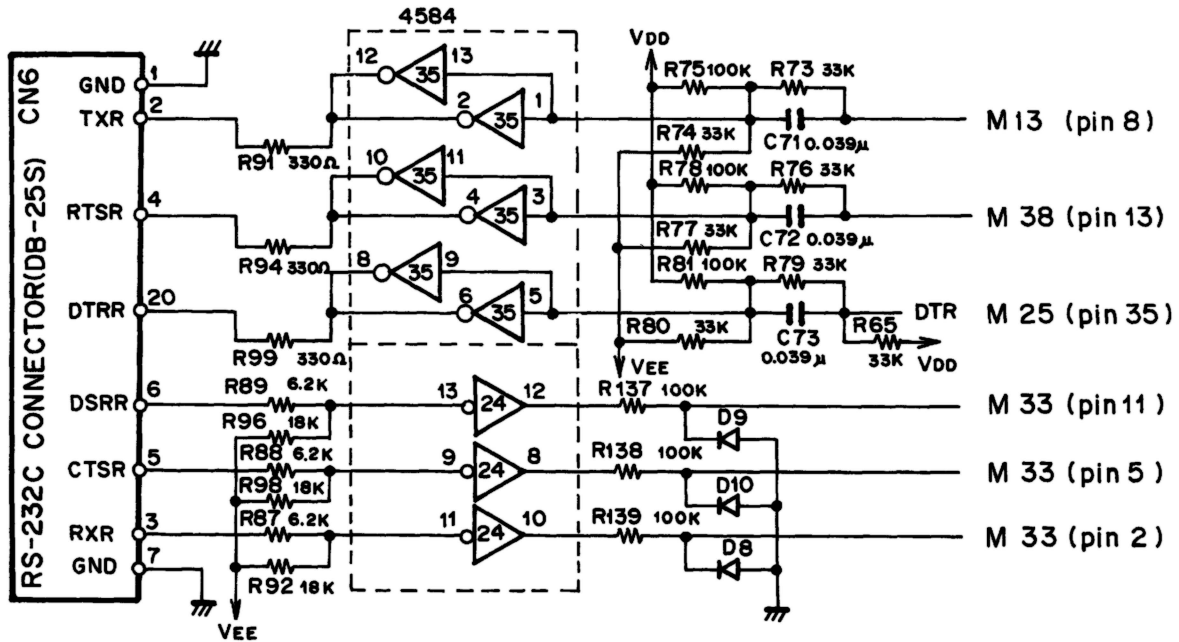


Figure 4-16. RS-232C Interface Circuit

MODEM IC

The Tandy 102 employs the IC MC14412 as a MODEM control device. This IC modulates/ demodulates data to be transmitted/received in accordance with frequencies suitable for originate or answer mode respectively.

The RXRATE and TYPE terminals of the MC14412 (M31) are pulled up to VDD. The baud rate is set to 300 bps and the U.S.Standard is selected. Since the ECHO and SELFTEST terminals are not needed, they are connected to ground.

The Q output (EN signal) of the M36 selected by bit 1 of the $\overline{Y2}$ port is input to the ENABLE terminal when the MODEM mode is selected.

In addition, the signal detected by the ORG/ANS switch is input to the MODE terminal, and it switches between the ORIGINATE mode or ANSWER mode.

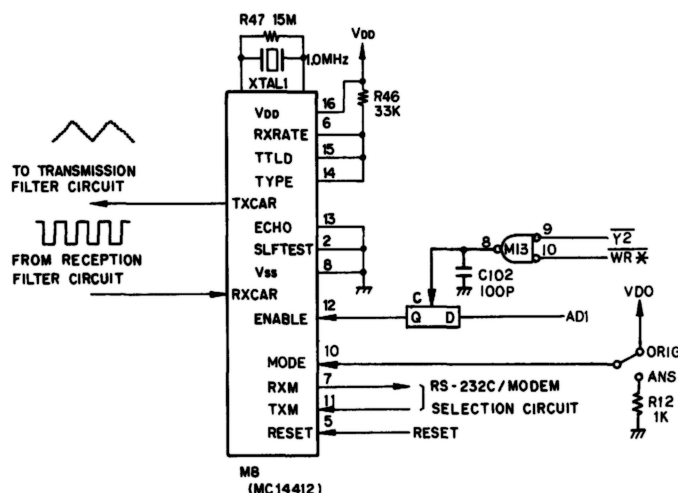


Figure 4-17. MODEM IC and Peripheral Circuit

Transmission Filter Circuit

The DC component of the carrier output from the TXCAR terminal is removed by C61. The signal level is adjusted by the potentiometer VR2. The signal then passes through the transmission band-pass filter and is sent to the telephone line or the acoustic coupler.

The transmission filter circuit is composed of an active filter (consisting of an operation amplifier) and the intermediate frequency of the active filter is 1170 Hz for the originate mode, and 2125 Hz for the answer mode. They are changed by switching T4 ON or OFF.

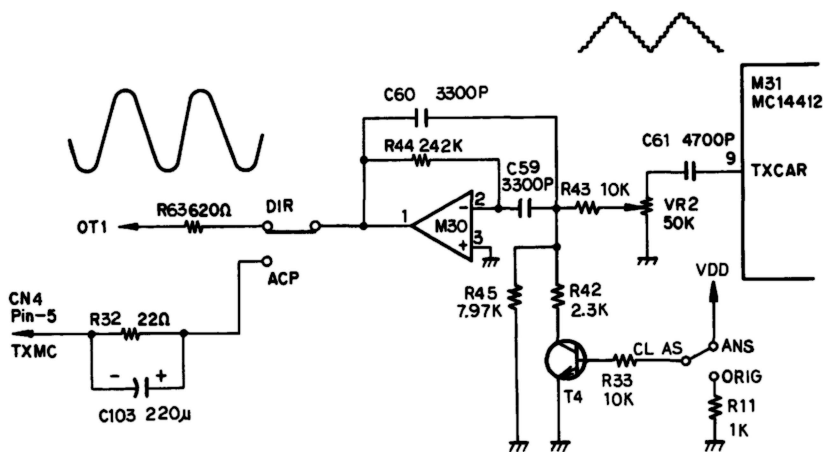


Figure 4-18. Transmission Filter Circuit

Reception Filter Circuit

As shown in Figure 4-19, the reception input signal is amplified when passing through coupling capacitor (C40), and amplified again as it passes through the 3-stage band-pass filter (composed of an active filter). The signal then passes through the comparator, and after being changed to a square wave, is input at the RXCAR terminal of the MC14412. Also, to check a carrier signal, this signal is input to the demultiplexer M33.

The intermediate frequencies of the 3-stage active filter are shown below. The switching of intermediate frequency for the originate and answer mode is accomplished by switching T2, T3 and T5 ON or OFF according to the ORG/ANS switch position, thus changing the input resistance of the filters.

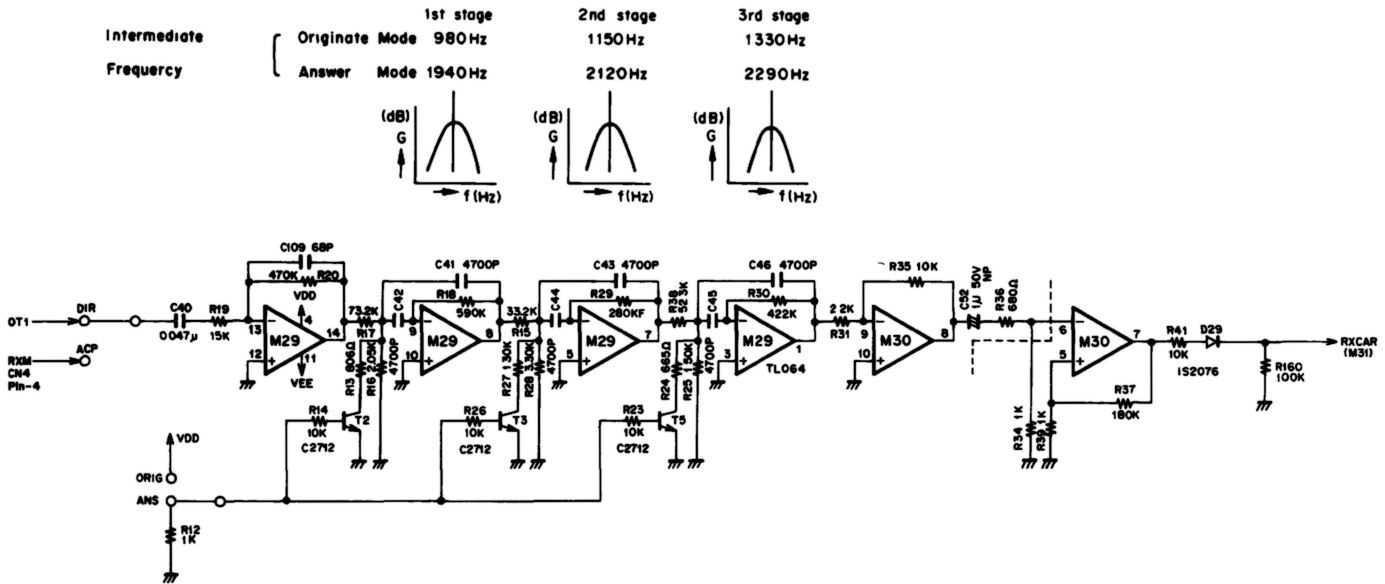


Figure 4-19. Reception Filter Circuit

Modem Transmitting Level Adjustment

1. Set the DIR/ACP switch to the DIR position.
2. Connect a 600-ohm dummy load between pin-3 (RXMD) and pin-7 (TXMD) of the MODEM connector (CN4).
3. Connect an AC voltmeter across the above dummy load.
4. Set up the Tandy 102 in BASIC mode and enter the following command to generate the carrier signal:

OUT 178,47 [ENTER]

OUT 168,02 [ENTER]

5. Adjust VR2 so as to read -14 to -17 dBm on the AC voltmeter for both ANS and ORIG modes.

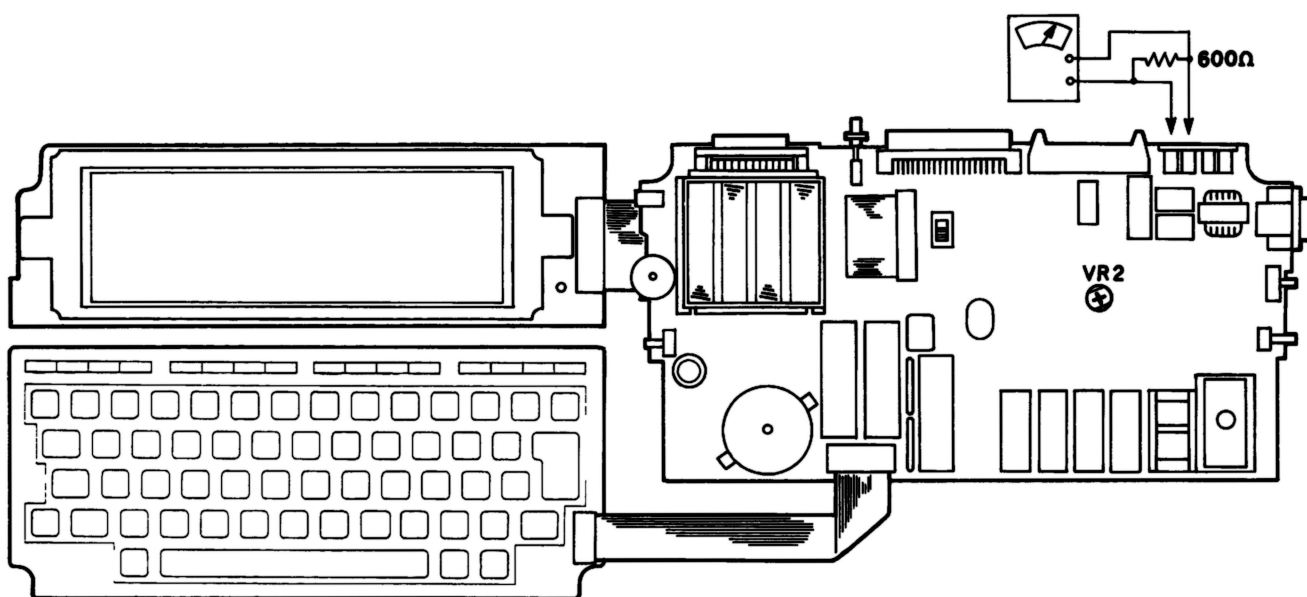


Figure 4-20. MODEM Adjustment

MODEM Connector Interface Circuit

When the acoustic coupler is used, the transmission and reception signals are directly connected to the connector (TXM, RXM). When the MODEM cable is used, they are connected to the secondary side of the driver transformer. The primary side of this transformer is connected to the telephone line via the connector (TXMD, RXMD).

The ACP/DIR switch is used in the MODEM mode, relay RY3 separates the telephone receiver audio signal (TL) to prevent interference. RY2, another relay, separates the MODEM circuit and the telephone at the conclusion of use in the MODEM mode and is also used as an automatic dialer for the pulse-type telephone line.

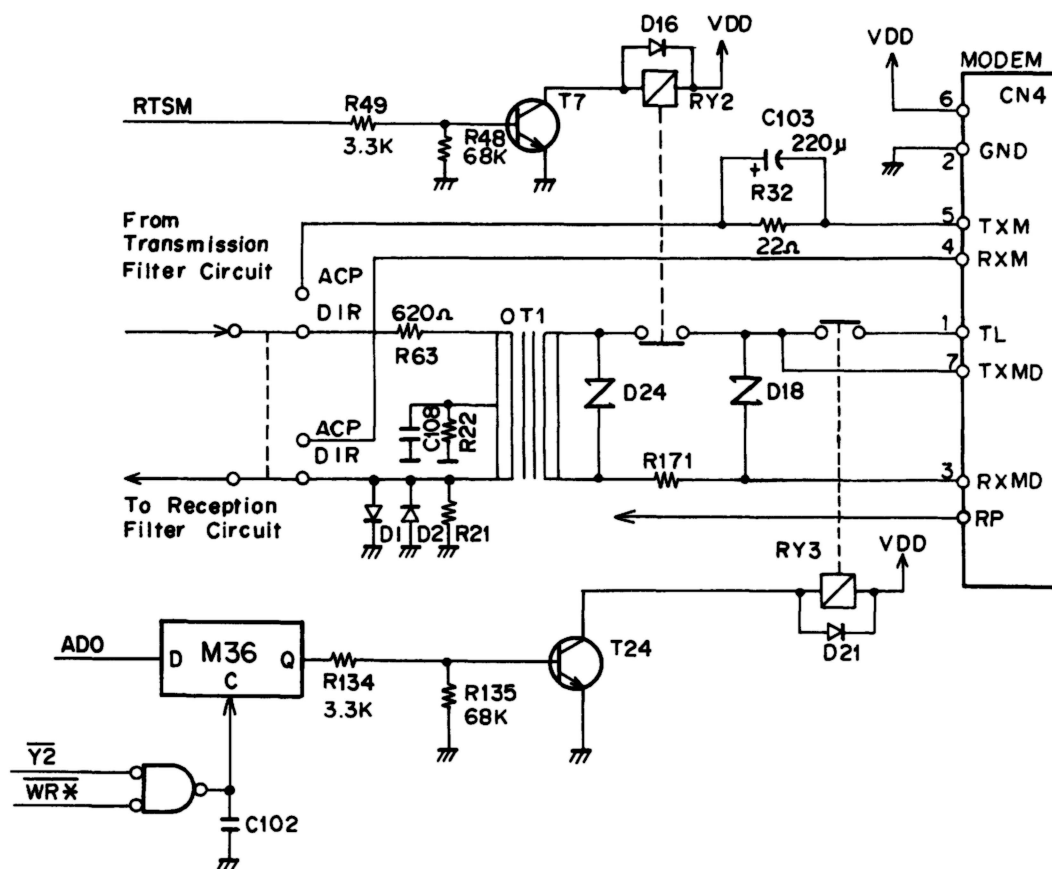


Figure 4-21. MODEM Connector Interface Circuit

LCD

The LCD used in the Tandy '102 is composed of electrodes in a matrix arrangement (64 common signals and 480 segment signals) This part is subdivided into the following three sections:

- LCD Common Driver
- LCD Segment Driver
- LCD Waveform

For a more detailed description of how the LCD operates and its basic construction, refer to Appendix C of this manual.

LCD Common Driver (HD44103)

The Tandy 102 uses two common driver ICs: M11 and M12. M11 controls the upper half of the LCD screen and M12 controls the lower half of the LCD screen. M11 and M12 are cascade connected, and a 1/32-duty backscan signal is made. By using C5 and R10 connected to the C and R terminals of M11, a timing signal is generated, which controls M12. M11 can be considered to be the master IC and M12 the slave.

The FRM signal defines the periodic frequency of one-screen display, and determines 70 Hz for the Tandy 102.

The MB signal is used for changing the driver signal to AC, because the continuous application of DC to the LCD would shorten the LCD element life.

The CL1 signal is used for the shift clock of the internal shift register.

The $\phi 1$ and $\phi 2$ signals are the clock signals for the HD44102 RAM operation.

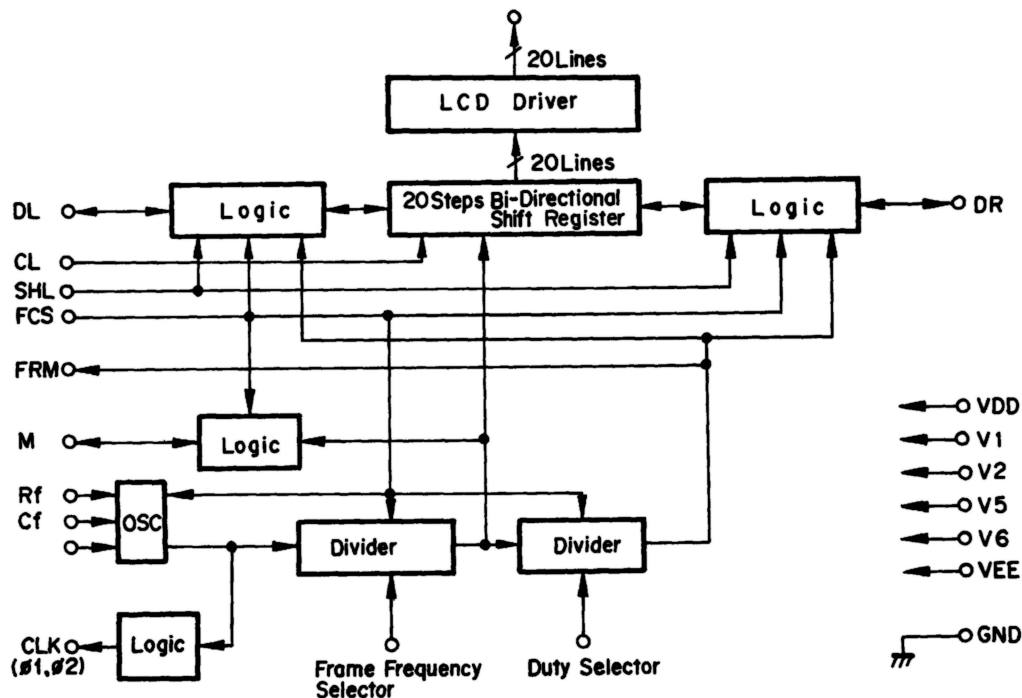


Figure 4-22. HD44103 Internal Logic Diagram

LCD Segment Driver (HD44102)

M1-M10 (HD44102) on the LCD PCB are segment driver ICs that cause the display data sent from the main PCB to be memorized in the built-in RAM and automatically generate the LCD drive signal. One bit of data from the built-in RAM corresponds to one dot of illumination or non-illumination on the display. The driver outputs are 50 lines.

The transfer of the display data is accomplished by 8-bit parallel data. This IC has several types of commands. The D/I (H = data, L = command) signal distinguishes between commands and data. The Tandy 102 has 240 segments each (upper and lower), the segment driver outputs Y41-Y50 are not used. The power supplied to these ICs, in addition to VDD (+5V) and VEE (-5V), also includes V1-V6.

VDD and VEE are the power supplies which operate the IC logic. V1-V6 operate the LCD driver signals.

V1-V6 are made up by the resistance splitting of R1, R2, R3, R4 and R5. By passing through the operational amplifier M13, the output impedance of the power supply is lessened.

Capacitors C3, C4, C6, C7 and C8 augment the peak current during LCD illumination.

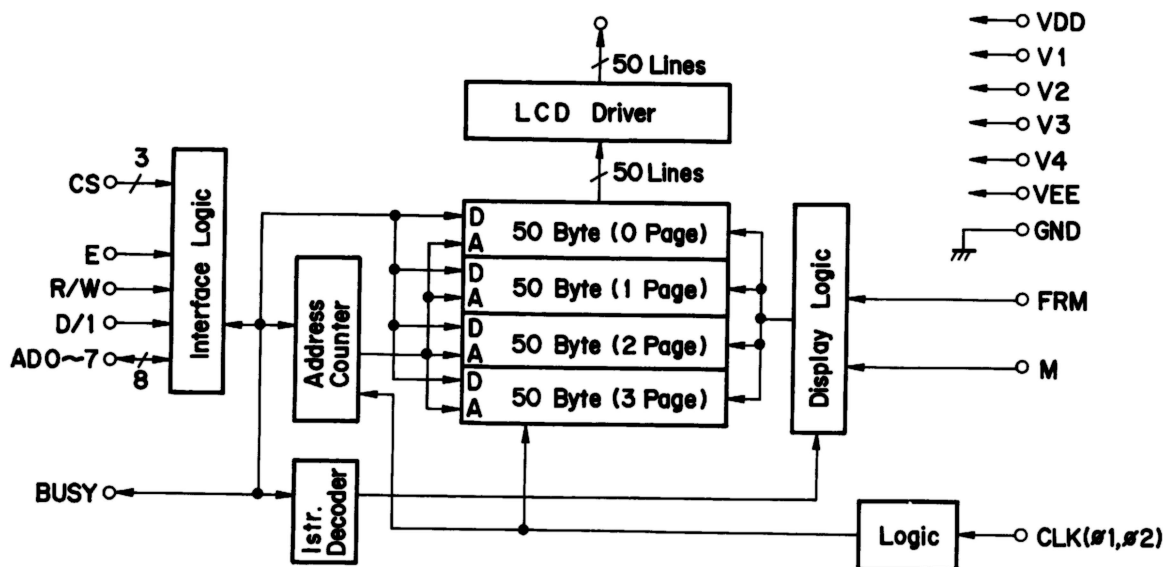


Figure 4-23. HD44102 Internal Logic Diagram

LCD Waveform

In order to drive the liquid-crystal element by the 1/32 duty line-sequential drive method, the LCD of the Tandy 102 makes sequential selection of the 32 scanning electrodes.

For each dot, the display signal passes through the signal electrode and is applied 32 times for one display.

At this point, the signal is necessary at each dot only one time. The signals for the other 31 times correspond to other dots on the same signal electrode.

The maximum voltage applied to common electrode and segment electrode is the potential difference between V1 and V2.

In addition, "a" is the bias coefficient which determines, from the standpoint of contrast, the maximum ratio between the illumination voltage and the non-illumination voltage.

When that ratio is the greatest in relation to the effective ON and OFF voltages, $a = 6.66$.

Thus, for V1, V2, V3, V4, V5 and V6:

$$V1 = VEE(-5V)$$

$$V2 = V \text{ (about 0-4V)}$$

$$V3 = 2/aV$$

$$V4 = (1-2/a)V$$

$$V5 = (1-1/a)V$$

$$V6 = a/aV$$

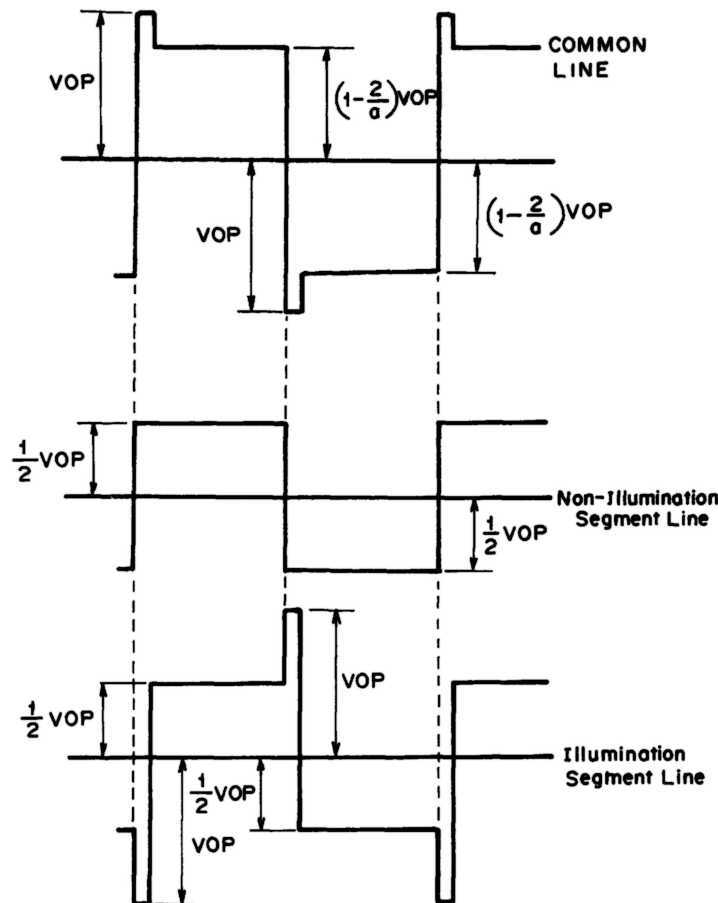


Figure 4-24. LCD Waveform

Power Supply Circuit

The Tandy 102 logic circuit uses +5V for VDD, -5V for VEE and +4 to +5V for VB. These voltages are supplied by the DC/DC converter. Also, the power supply circuit has the automatic power off function and reset circuit.

DC/DC Converter Circuit

OT2 is a converter transformer which oscillates T21 and T22 and generates voltages at the secondary side of the transformer. At the same time the power is switched ON, a very slight collector current flows to T21 and T22. As the current flowing through OT2 is increased, the voltage induced between pin 8 and pin 9 of the converter transformer causes pin 9 to be positive. The positive voltage is applied to the base of T22 passing through R126 and C81 to activate T21 and T22.

Fully charged, C81 stops the primary current. The secondary magnetic field begins to collapse, reversing the polarity of the induced voltage, causing pin 9 to be negative. By being applied to the base of T22 through C81, this voltage is used to turn OFF T21 and T22, as C81 discharges. Discharged C81 allows the transistor to turn ON again to repeat this cycle. The switching frequency is determined by R126 and C81.

The output of this circuit is derived from the secondary winding. VEE is from pin 9, rectified by D15, filtered by C85, and VDD is from pin 7, rectified by D13, filtered by C84.

Also, VDD is fed back to the base of T13 through zener diode D4 to maintain VDD of +5V.

Low Power Detection Circuit

The low power detection circuit illuminates an LED warning lamp when the battery voltage decreases. If it continues to decrease, the system power will be switched OFF just before the voltage becomes so low that the converter cannot operate.

There are about 20 minutes between the time when the LED lamp illuminates and the system is switched OFF.

Battery voltage is detected by splitting the resistance of R105, R108, R144 and R116. When the battery voltage (VR) becomes $4.2V \pm 0.1V$, T16 is switched OFF. T17 is switched ON, T19 is driven, and the LED illuminates.

When VL becomes $3.7V \pm$, T14 is switched OFF, T15 is switched ON, and the \overline{LPS} signal changes from H to L. This signal is inverted by M34 and fed to the TRAP terminal of the CPU. If the CPU acknowledges this signal, it sends the PCS signal passing through the PB4 of the PIO after the internal operations.

When the PCS becomes H, the Q output of M28 becomes H, T20 operates and the oscillation of the converter is stopped.

If there is no operation for 10 minutes or more (awaiting a command for 10 minutes or more), the PCS is output from the PB4 of the PIO.

When the power switch is switched OFF, T18 is switched OFF, the RESET terminal of M28 becomes H and oscillation is resumed by switching the power switch ON. If, however, the power is reduced by the PCS signal, a battery replacement is necessary.

RESET Circuit

This circuit supplies the \overline{RESET} signal and also the RAM RST signal as the protecting signal for the contents of the RAM when the power decreases. C78 and R103 delay the introduction of input power so that T11 is switched ON and T10 is switched OFF after VDD is activated, with the result that the \overline{RESET} signal changed from L to H. In the same way, the RAM RST signal is generated by T9 and changes from H to L. Thermistor TH2 suppresses the \overline{RESET} signal fluctuations due to temperature.

T25 receives the signal from the Q terminal of M28 during automatic power OFF, short-circuiting both ends of C78, and resets the system. The \overline{RESET} signal is active L and the RAM RST signal is active H.

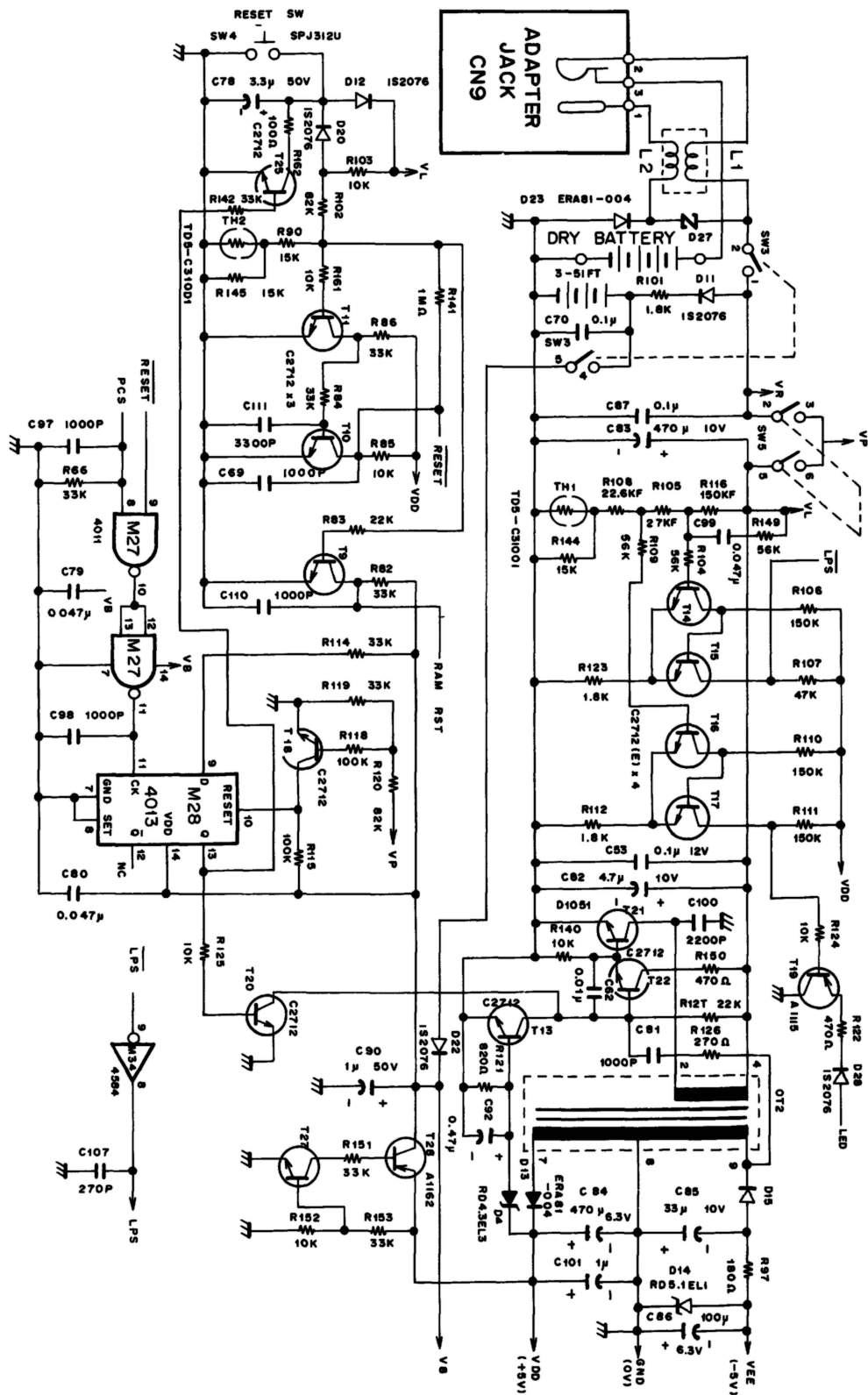


Figure 4-25. Power Supply and Reset Circuit

V. TROUBLESHOOTING

General Guidance

How to Make Use of This Section

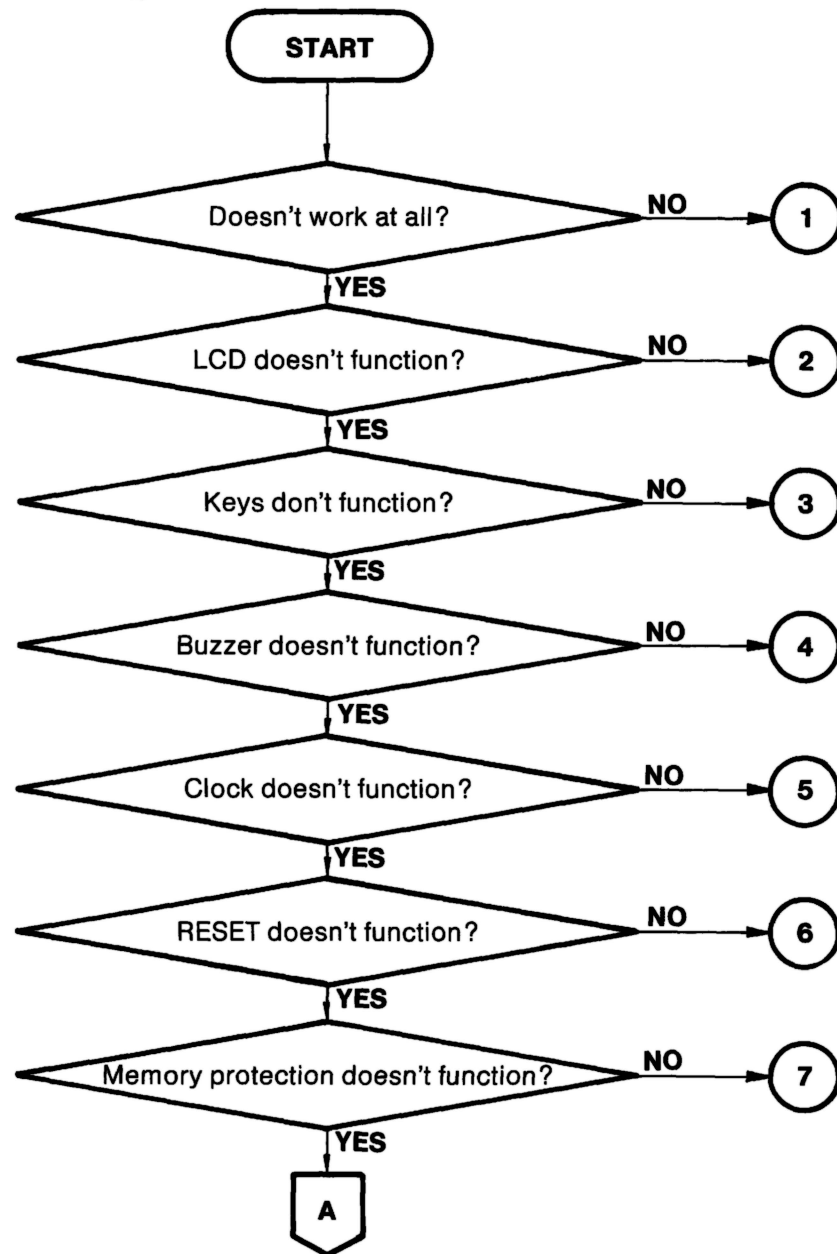
If you have a problem or have to repair the Tandy 102, this section will be very helpful to you.

If the location or condition of the malfunctions are clear, for instance, the buzzer does not function, refer to the flowchart in the TROUBLESHOOTING GUIDE and find the number circled. Then, you will be able to find the necessary information, such as corresponding ICs and transistors, for malfunction repair.

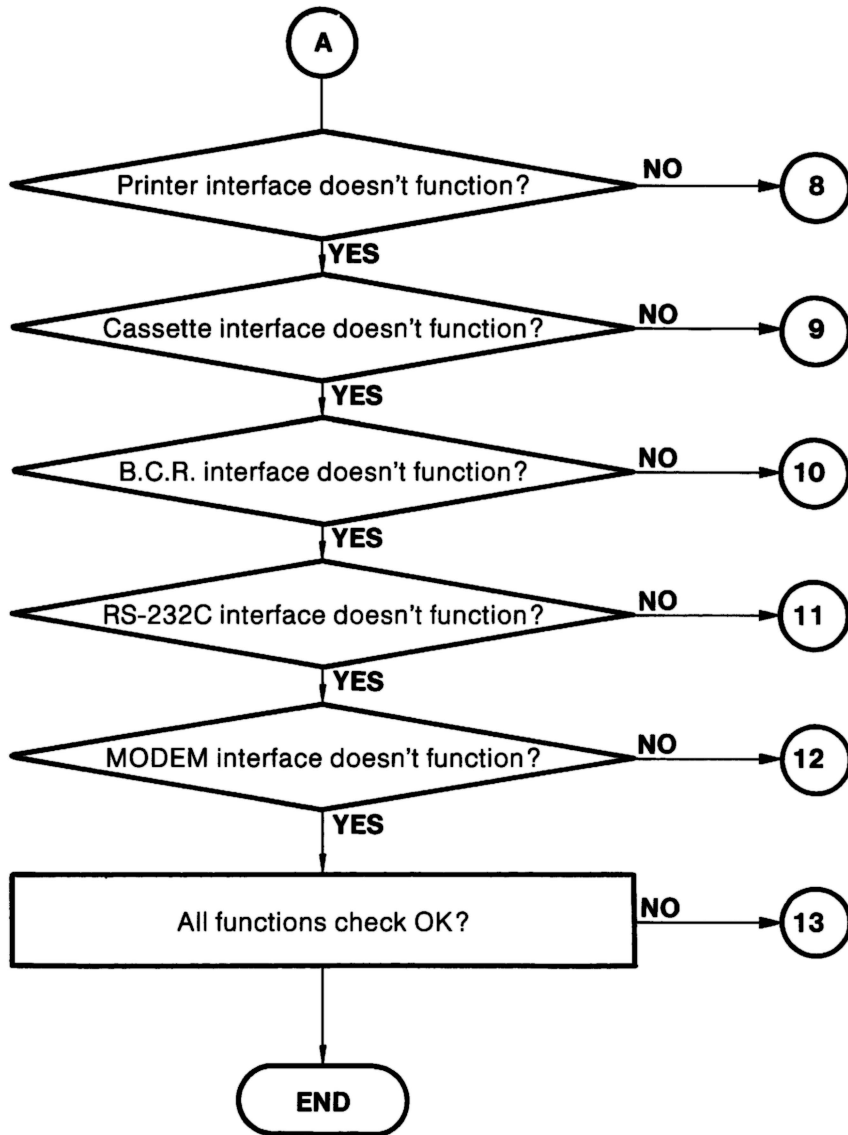
After you complete the malfunction repair, re-check each functional item according to the CHECK LIST.

You can make use of the CHECK LIST even if the location and condition of the malfunction are not clear.

Troubleshooting Guide

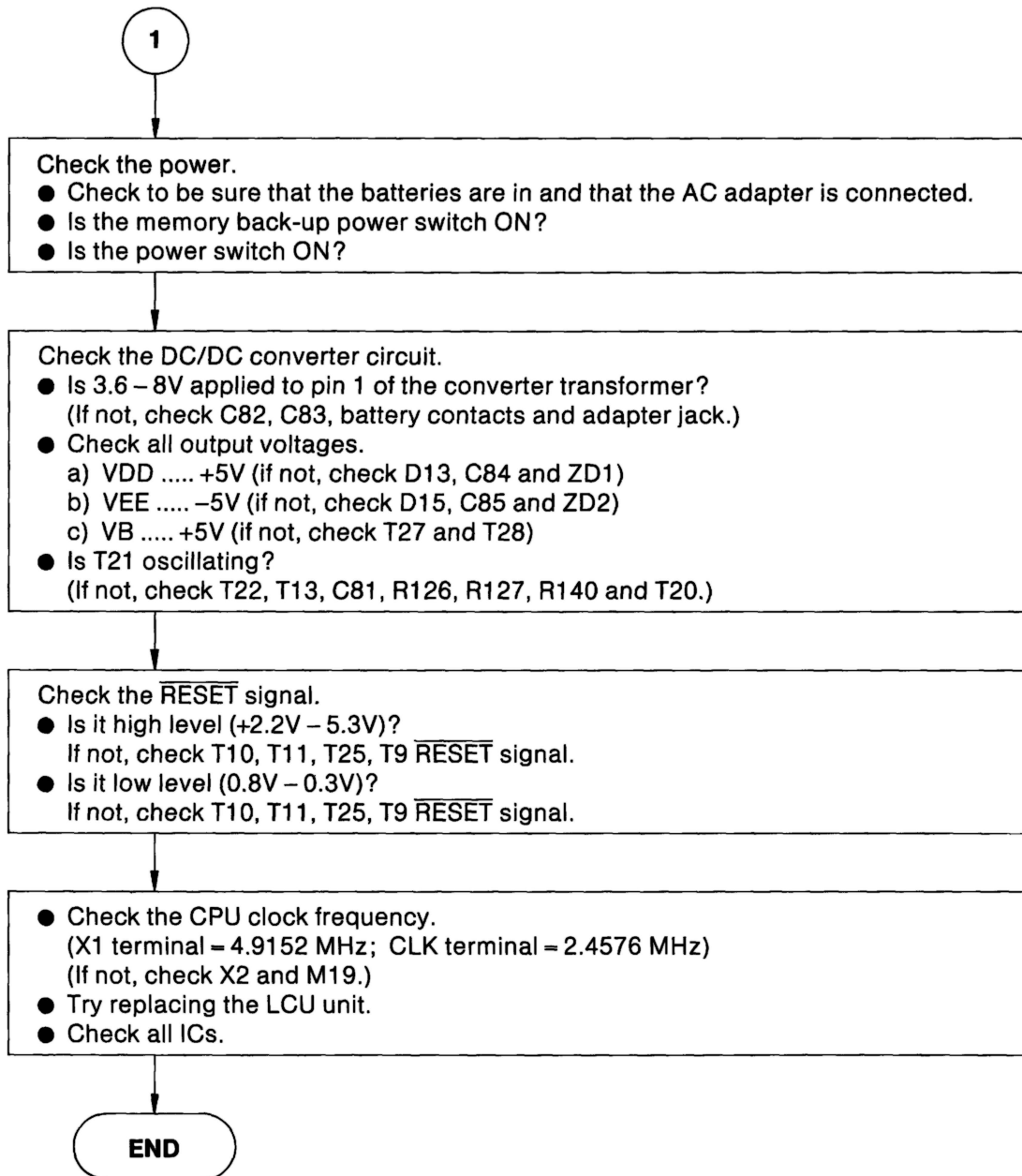


TO NEXT PAGE

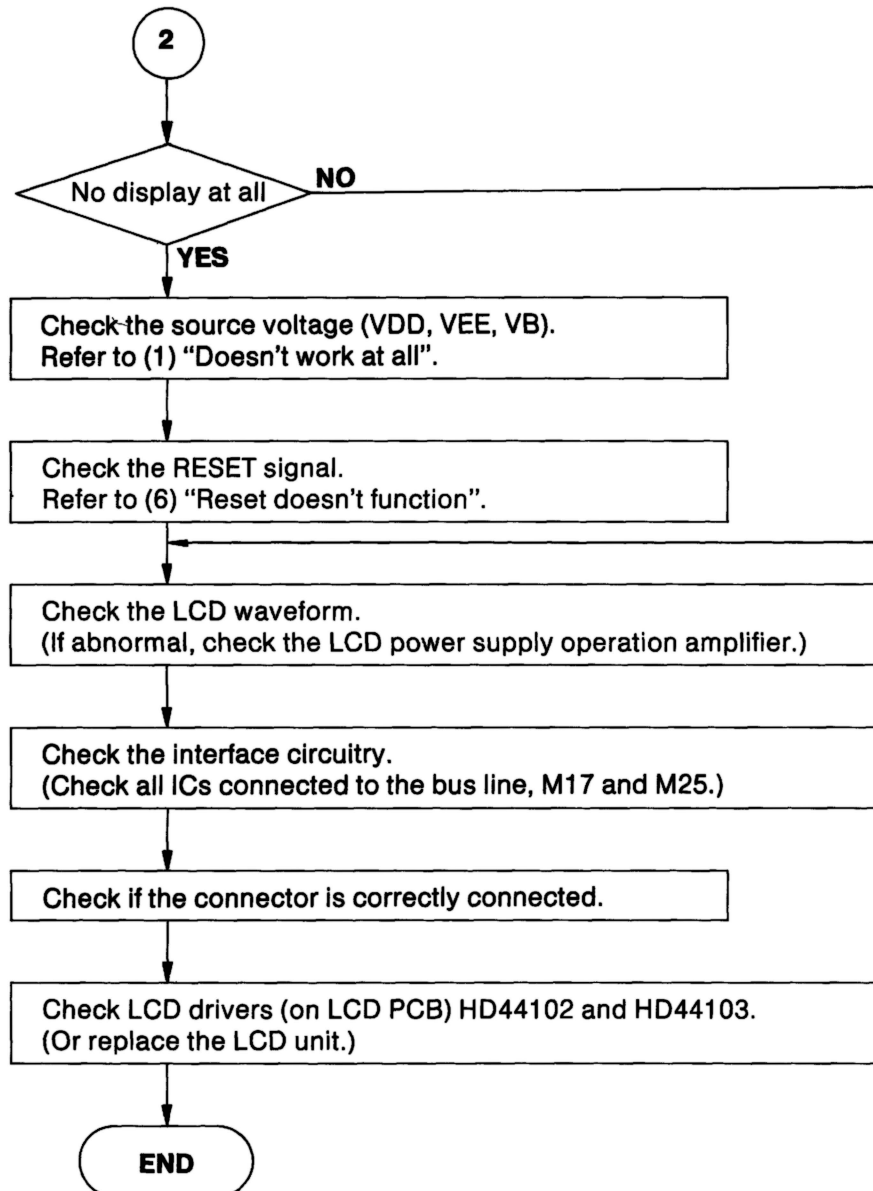


Checking Procedure

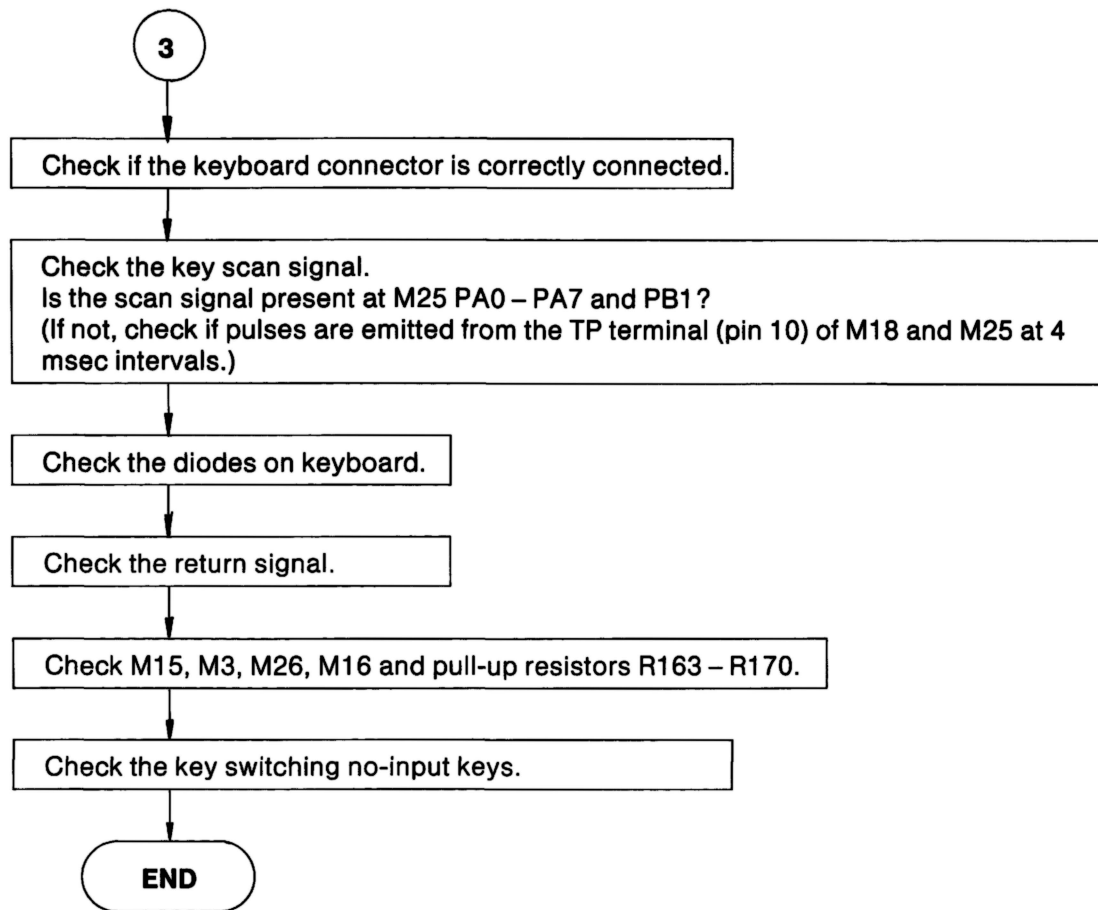
1. Doesn't work at all



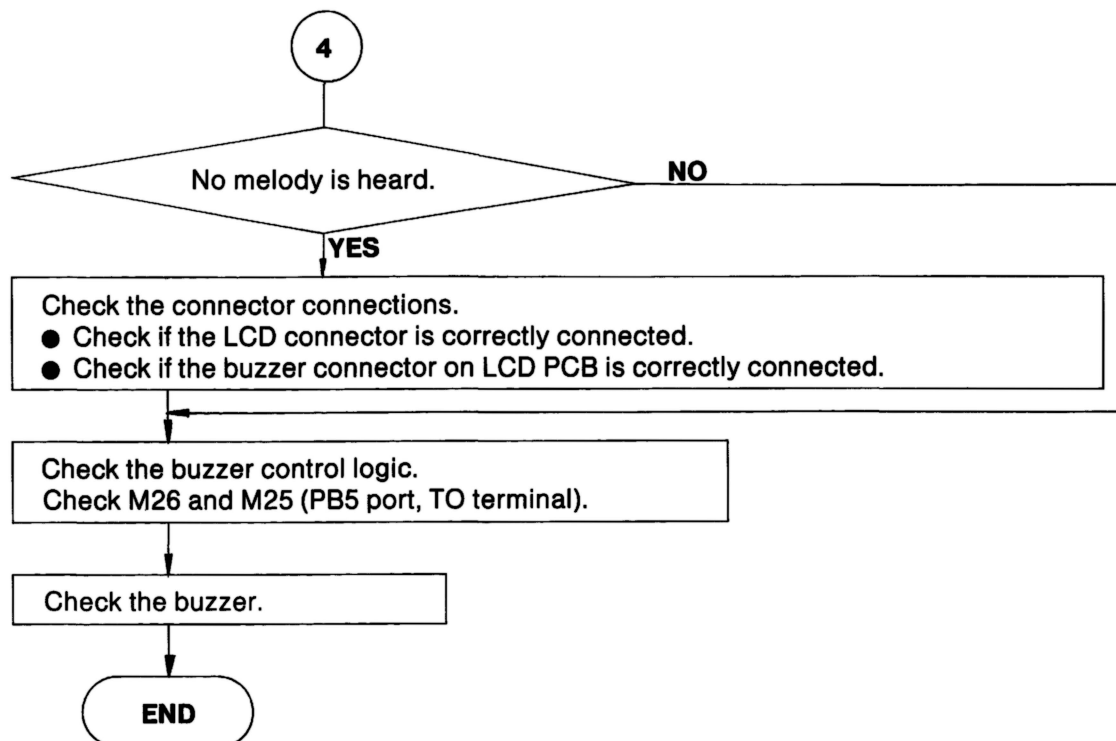
2. LCD doesn't function



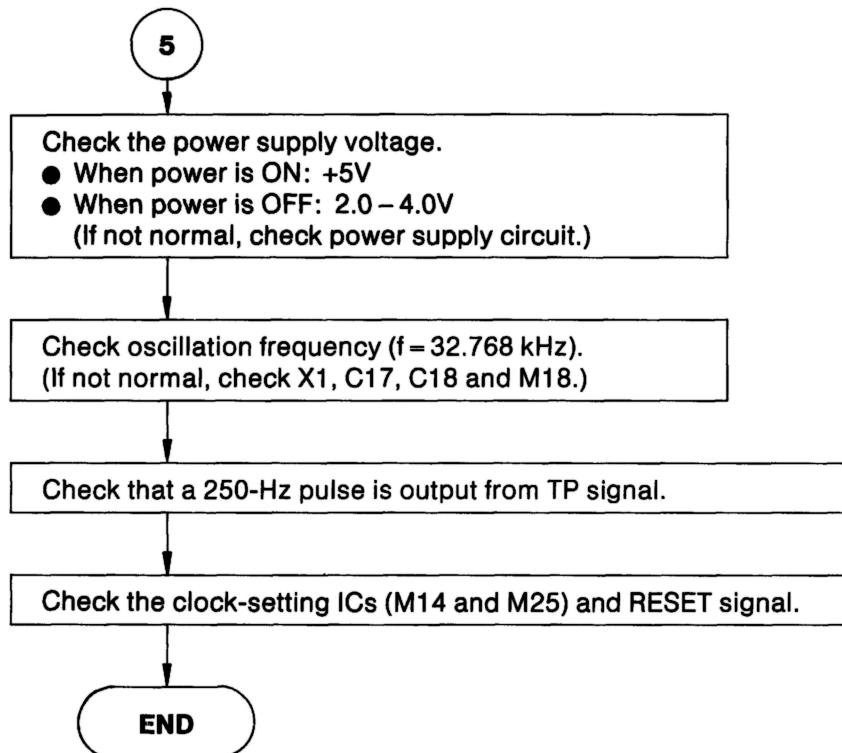
3. Key doesn't function



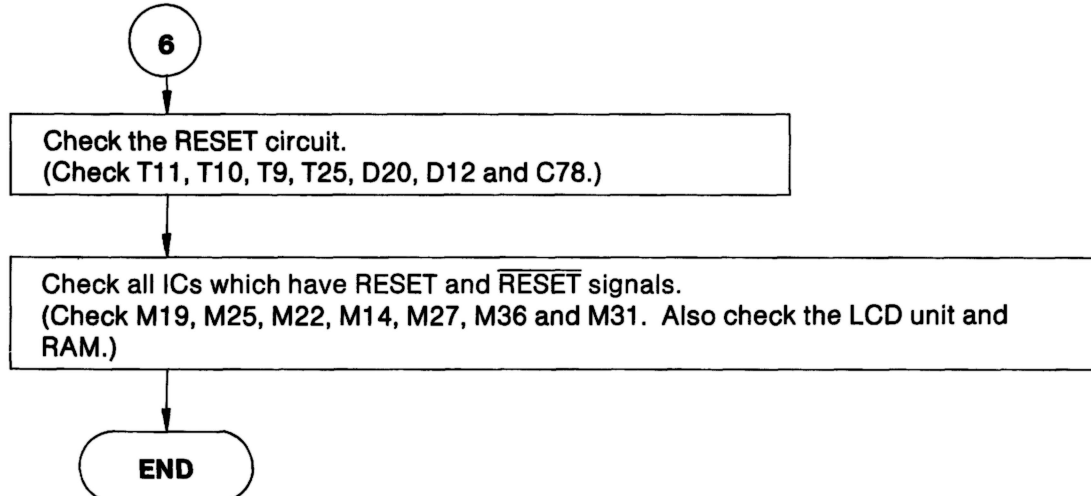
4. Buzzer doesn't function



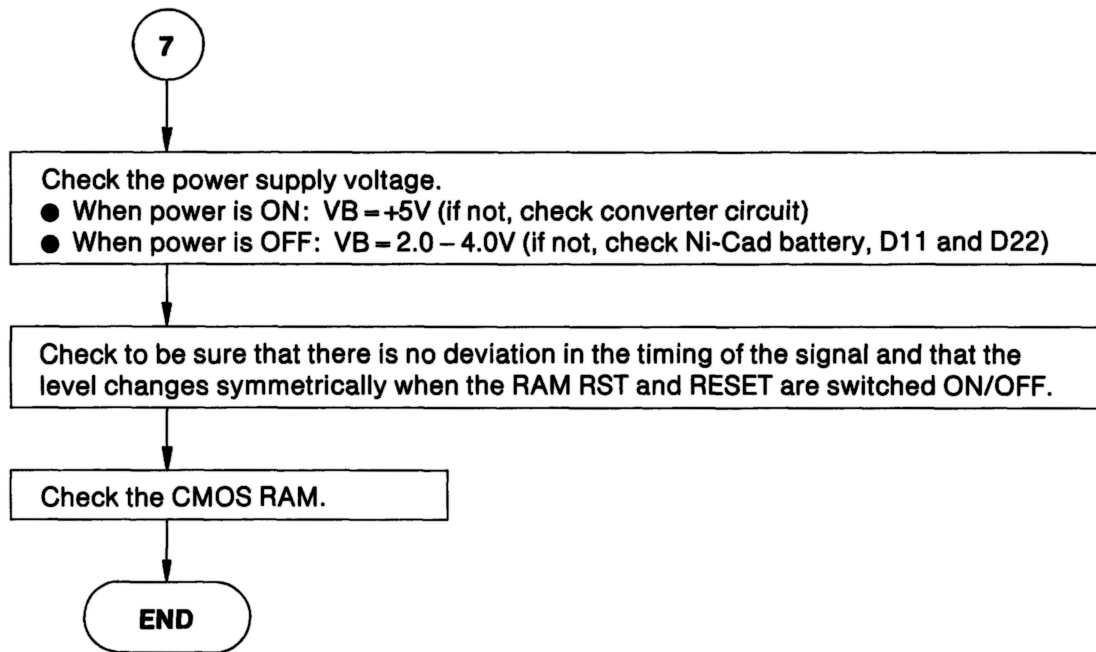
5. Clock doesn't function



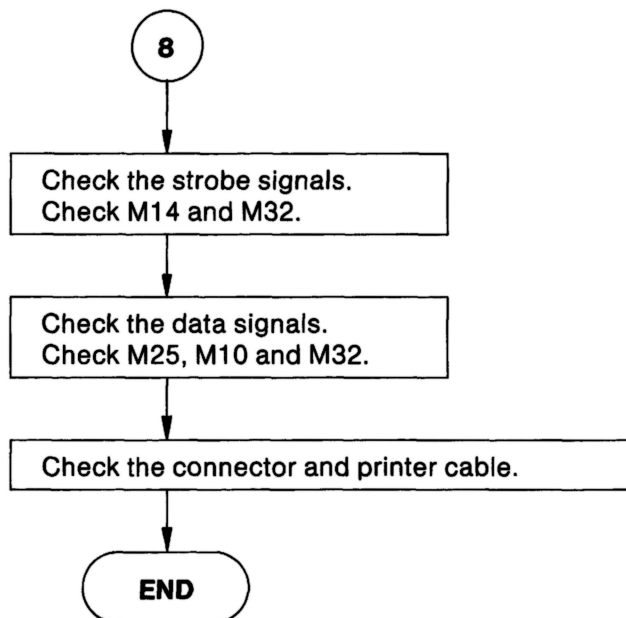
6. Reset doesn't function



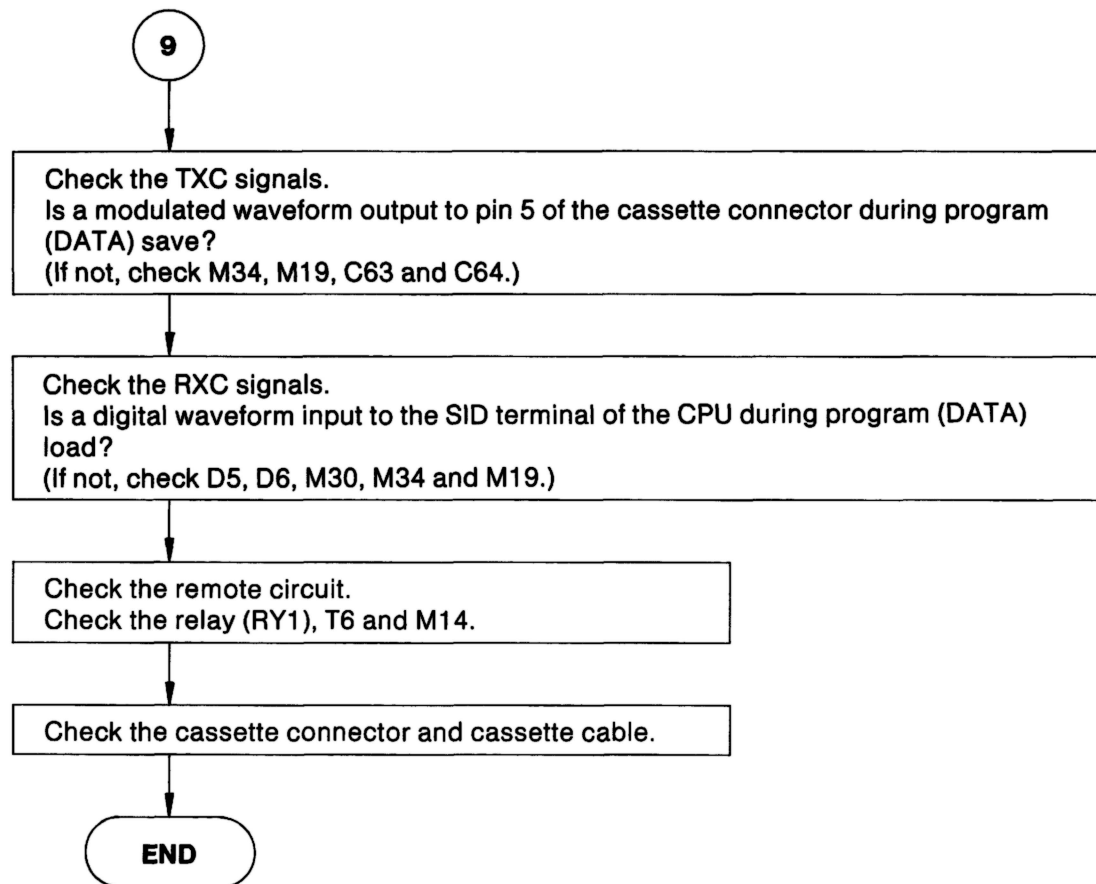
7. Memory protection doesn't function



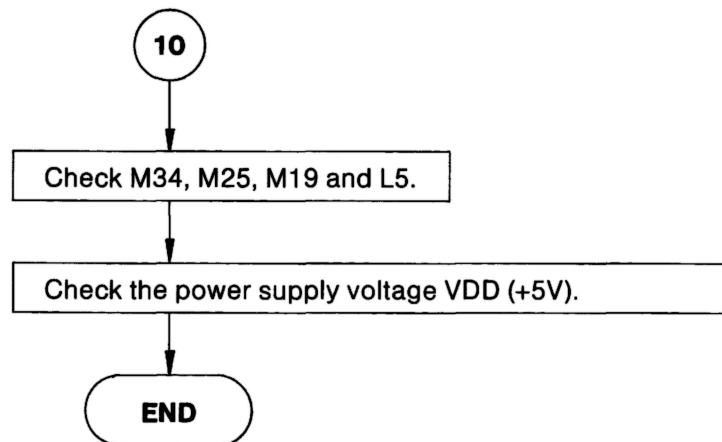
8. Printer interface doesn't function



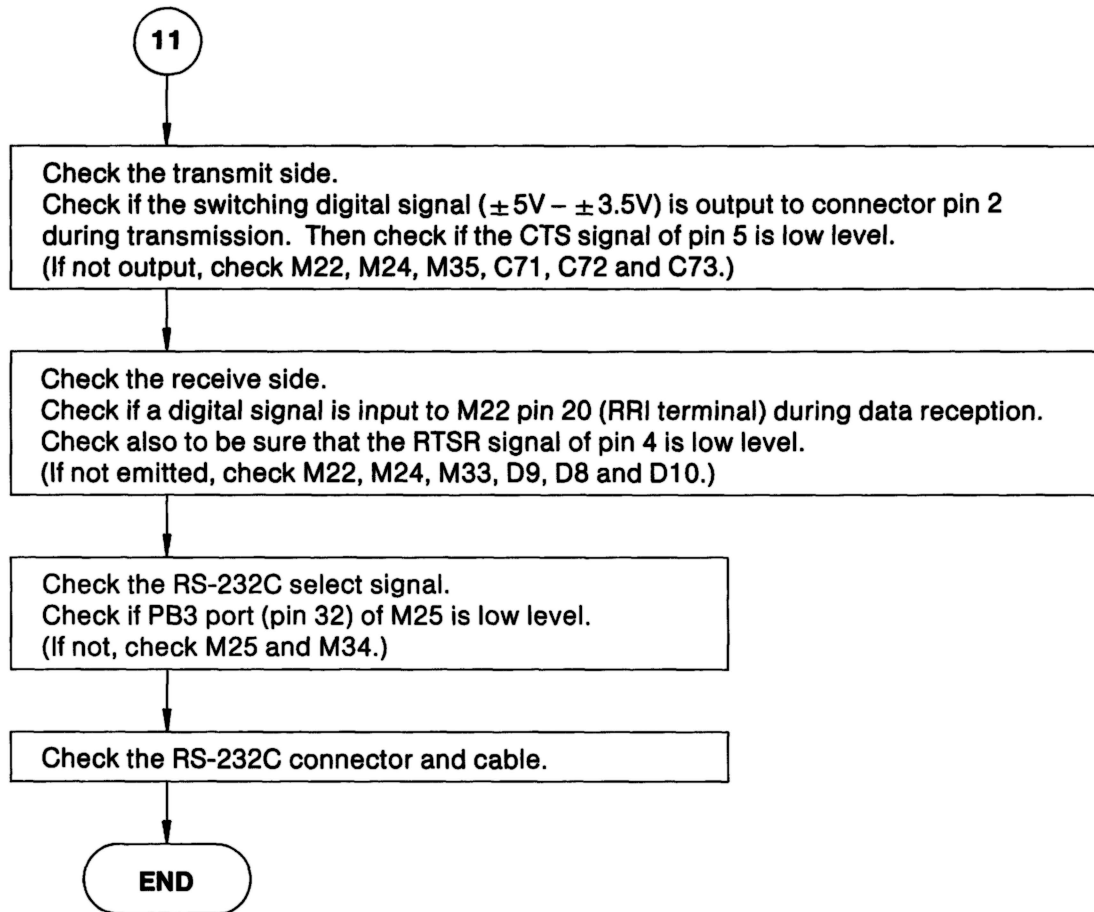
8. Cassette interface doesn't function



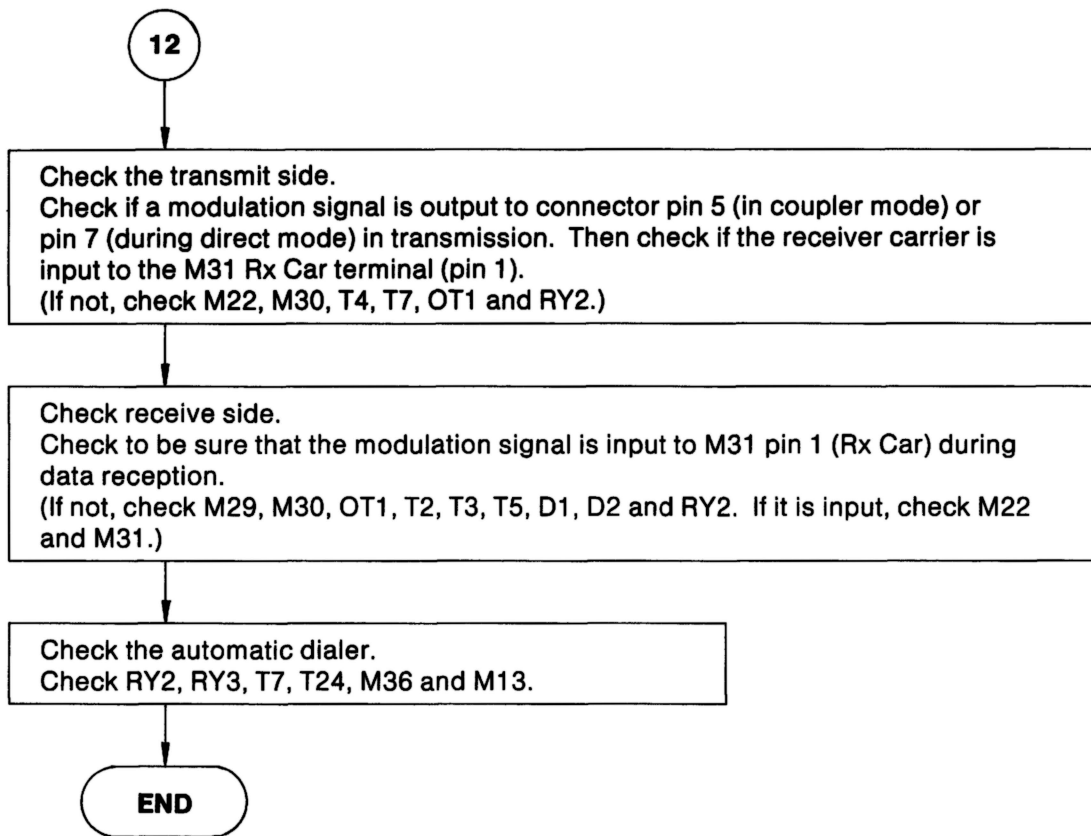
10. B.C.R. interface doesn't function



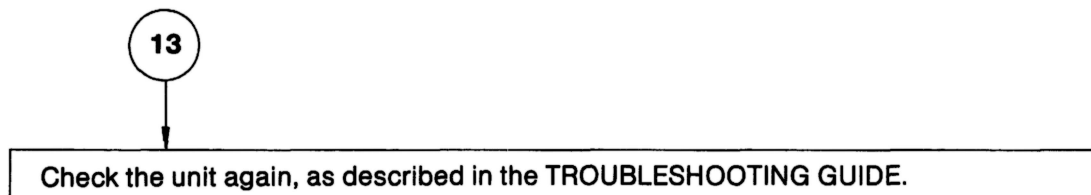
11. RS-232C interface doesn't function



12. Modem interface doesn't function



13. All functions check ok?



Check List

After completing all repairs and adjustments, check all functions according to the Test Program as shown below. A model 100 diagnostics tape available through Radio Shack can also be used. Before beginning the checking, initialize the RAM contents by performing a cold start. Refer to "(4) Reset function test".

(1) Buzzer and LCD check (in BASIC mode)

```
10 FOR I = 0 TO 255
20 PRINT CHR$(I);
30 NEXT I
40 END
```

After 1 beep and the LCD display clears, all characters are displayed.

(2) Clock test (in BASIC mode)

(a) Setting the year, month, date, day, hour, minute and second:

Year, month, date setting: Date\$ = "MM/DD/YY"

Day setting: DAY\$ = "day" (example: Sunday = SUN)

Hour, minute, second setting: TIME\$ = "HH: MM: SS"

(b) Confirmation of set data

Return to the menu by executing the MENU command. Then, check to be sure that the calendar data changes to set data.

(3) Key board test

Refer to the character code table in Appendix B and check that all keys can be input.

(4) Reset function test (memory protection test)

(a) Warm start

Press the RESET switch on the rear of the case or switch the POWER switch to ON, and check that initialization is made. Also check that the saved USER files are not erased.

(b) Cold start

While pressing the CTRL and PAUSE keys, press the RESET switch and check that all USER files are erased.

(5) Printer Interface test (in BASIC mode)

Input the characters to be printed out on the LCD display. When the hard copy key PRINT is pressed, the displayed characters will all be printed out.

(6) Cassette Interface test (in BASIC mode)

Input a suitable program, save it on cassette (by CSAVE "file name"), and then read out the saved program (by CLOAD "file name") and check it.

(7) RS-232C and MODEM tests.

Prepare two units and make the tests while referring to the section on communications in the Operation Manual.

VI. EXPLODED VIEW/PARTS LIST

Exploded View

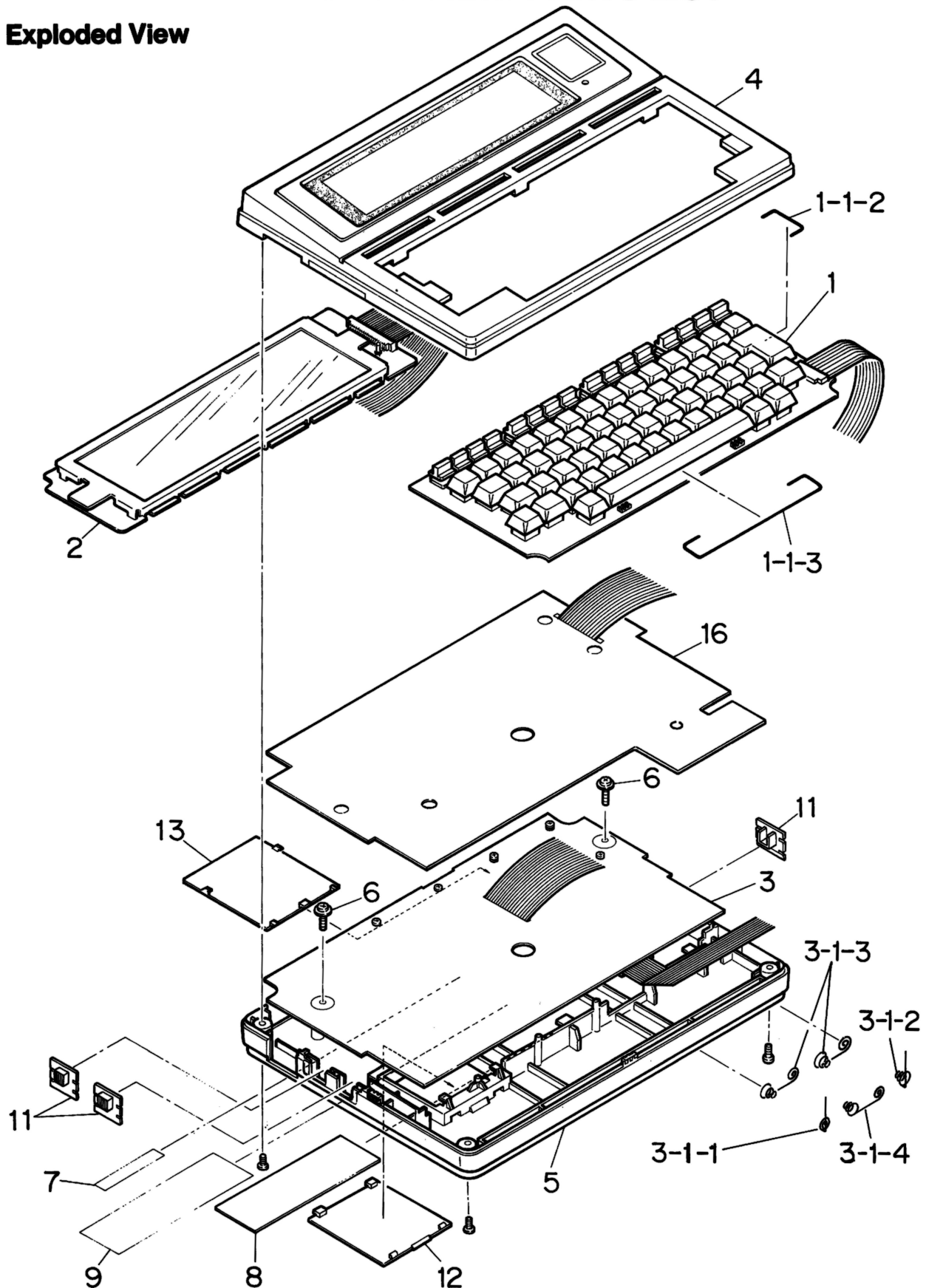


Figure 6-1. Exploded View

Electrical Parts List

Main PCB Assembly

Ref. No.	Description	RS Part No.	Mfr's Part No.
CAPACITORS			
C1-C4	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C5-C11	Ceramic	0.1 μ F / 25V / +80-20%	CD-104ZFCP CFPC104ZF%
C12-C16	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C17, C18	Ceramic	20pF / 50V / \pm 10%	CD-200KJCP CFPD200KP%
C19	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C20-C27	Ceramic	82pF / 50V / \pm 10%	CD-820KJCP CFPD820K0%
C28	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C29, C30	Ceramic	10pF / 50V / \pm 0.5%	CFPD100DC%
C31	Ceramic	0.1 μ F / 25V / +80-20%	CD-104ZFCP CFPC104ZF%
C32-C35	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C36	Ceramic	0.1 μ F / 50V / \pm 10%	CD-104KJCP CFPD104ZF%
C37	Ceramic	0.1 μ F / 25V / +80%-20%	CD-104ZFCP CFPC104ZF%
C38	Ceramic	100pF / 50V / \pm 10%	CD-101KJCP CFPD101K0%
C39	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C40	Mylar *	0.047 μ F / 50V / \pm 5%	CC-473JJMP CQMB473JTH
C41-C46	Poly Film	4700pF / 100V / \pm 1%	CC-472FLGP CQPC472FEN
C47, C48	Ceramic	0.1 μ F / 25V / +80-20%	CD-104ZFCP CFPC104ZF%
C49, C50	Electrolytic	10 μ F / 16V / \pm 20%	CC-106MDAP CEVD100ALX
C51	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C52	Electrolytic	1 μ F / 50V / \pm 20%	CC-105MJAP CEVG010NLX
C53	Ceramic	0.1 μ F / 25V / +80-20%	CD-104ZFCP CFPC104ZF%
C54, C55	Electrolytic	10 μ F / 16V / \pm 20%	CC-106MDAP CEVD100ALX
C56-C58	Ceramic	0.1 μ F / 25V / +80-20%	CD-104ZFCP CFPC104ZF%
C59, C60	Mylar	3300pF / 50V / \pm 5%	CC-332JJMP CQMB332JTH
C61	Mylar	4700pF / 50V / \pm 5%	CC-472JJMP CQMB472JTH
C62	Ceramic	0.01 μ F / 50V / \pm 10%	CD-103KJCP CFPD103KB%
C63	Mylar	0.1 μ F / 50V / \pm 10%	CC-104KJMP CQMB104KTH
C64	Mylar	0.047 μ F / 50V / \pm 10%	CC-473KJMP CQMB473KTH
C65-C67	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C68, C69	Ceramic	1000pF / 50V / \pm 10%	CC-102KJCP CFPD102KB%
C70	Ceramic	0.1 μ F / 25V / +80%-20%	CD-104ZFCP CFPC104ZF%
C71-C73	Mylar	0.039 μ F / 50V / \pm 10%	CC-393KJMP CFPD393KB%
C74	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C75-C77	Electrolytic	47 μ F / 16V / \pm 20%	CC-476MDAP CEVD470NLX
C78	Electrolytic	3.3 μ F / 50V / +75%-10%	CC-335XJAP CEVG3R3ALX
C79, C80	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C81	Ceramic	1000pF / 50V / \pm 10%	CC-102KJCP CFPD102KB%
C82	Electrolytic	4.7 μ F / 25V / \pm 20%	CC-475MFAP CEVE4R7ALX
C83	Electrolytic	470 μ F // 16V / +30-10%	CC-477RCAP CEVD471UMN
C84	Electrolytic	470 μ F / 6.3V / +30%-10%	CC-477BBAP CEVB471ALN
C85	Electrolytic	33 μ F / 10V / \pm 20%	CC-336MCAP CEVC330ALX
C86	Electrolytic	100 μ F / 6.3V / \pm 20%	CC-107MBAP CEVB101ALX
C87	Ceramic	0.1 μ F / 25V / +80-20%	CD-104ZFCP CFPC104ZF%
C88-C89	Not used		
C90	Electrolytic	1 μ F / 50V / \pm 20%	CC-105MJAP CEVG010ALX
C91	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C92	Electrolytic	0.047 μ F / 50V / \pm 20%	CC-474MJAP CEVGR47ALX
C93	Not used		
C94	Ceramic	1000pF / 50V / \pm 10%	CC-102KJCP CFPD102KB%
C95, C96	Not used		
C97, C98	Ceramic	1000pF / 50V / \pm 10%	CC-102KJCP CFPD102KB%
C99	Ceramic	0.047 μ F / 50V / +80-20%	CD-473ZJCP CFPD473ZF%
C100	Ceramic	2200pF / 50V / \pm 10%	CD-222KJCP CFPD222KB%
C101	Not used		
C102	Ceramic	100pF / 50V / \pm 10%	CD-101KJCP CFPD101K0%
C103	Electrolytic	221 μ F / 10V / \pm 20%	CC-227MCAP CEVC221ACX

* Mylar is a registered trademark of E. I. Du Pont de Nemours and Company.

Ref. No.	Description	RS Part No.	Mfr's Part No.
C104	Ceramic 0.01 μ F/50V/ \pm 10%	CD-103KJCP	CFPD103KB%
C107	Ceramic 270pF/50V/ \pm 10%	CD-271KJCP	CFPD271K0%
C108	Mylar 5600pF/50V/ \pm 10%	CC-562KJMP	QOMB562KTH
C109	Ceramic 68pF/50V/ \pm 10%	CD-680KJCP	CFPD680K0%
C110	Ceramic 1000pF/50V/ \pm 10%	CC-102KJCP	CFPD102KB%
C111	Ceramic 3300pF/50V/ \pm 10%	CD-332KJCP	CFPD332KB%
CONNECTORS			
CN1	Jack, Junction to Keyboard	AJ-0010	YJF18S016Z
CN2	Jack, Junction to BCR	AJ-7342	YJF09S039Z
CN3	Jack, Junction to CMT	AJ-7340	YJF08S033Z
CN4	Jack, Junction to MODEM	AJ-7341	YJF08S034Z
CN5	Jack, Junction to Printer	AJ-7345	YJF26S010Z
CN6	Jack, Junction to RS-232C	AJ-7344	YJF25S019Z
CN7	Jack, Junction to LCD	AJ-0013	YJF30S012Z
CN8	Jack, Junction to System Bus	AJ-7634	YJF40S015Z
CN9	Jack, Junction to AC Adapter	AJ-7627	YJB03S007Z
DIODES AND SURGE ABSORBERS			
D1,D2	Diode, Silicon 1S2076	ADX-1763	QDSS2076#B
D3	Not used		
D4	Diode, Zener RD4.3EL3	DX-0064	QDZ4R3ELCA
D5-D12	Diode, Silicon 1S2076	ADX-1763	QDSS2076#B
D13	Diode, Silicon HRP22		QDSHRP22XB
D14	Diode, Zener RD5.1EL1	DX-0065	QDZ5R1ELAA
D15-D17	Diode, Silicon 1S2076	ADX-1763	QDSS2076#B
D18	Surge Absorber ERZ-C10DK361	ADX-1864	QNHDK361AN
D19	Not used		
D20-D22	Diode, Silicon 1S2076	ADX-1763	QDSS2076#B
D23	Diode, Silicon HRP22		QDSHRP22XB
D24	Surge Absorber ERZ-C10K220	ADX-1863	QNDDK220AN
D25,D26	Not used		
D27	Surge Absorber SNR-7D18L	ADX-1862	QNB7D18LAD
D28,D29	Diode, Silicon 1S2076	ADX-1763	QDSS2076#B
COILS			
L1,L2	Choke 10 μ H/500mA/Axial	ACA-8286	LF100KE04Y
L3,L4	RF (with beads) B-01AT		LBPDG5205A
INTEGRATED CIRCUITS			
M1	Hi-speed C-MOS, Latch TC40H373F	MX-2209	QQF40373TT
M2	Hi-speed C-MOS, Buffer TC40H245F	MX-2207	QQF40245TT
M3,M4	Hi-speed C-MOS, Buffer TC40H367F	MX-2208	QQF40367TT
M5	Hi-speed C-MOS, Decoder TC40H139F	MX-2204	QQF40139TT
M7-M9	C-MOS, RAM μ PD4364C or TC5565PL-15	MX-2210	QQ0D4364AA QQ005565AT
M10	Hi-speed C-MOS, Buffer TC40H367F	MX-2208	QQF40367TT
M12	C-MOS, Masked ROM HN613256PD-91	MX-2213	QQ061325QB
M13	Hi-speed C-MOS, OR Gate TC40H032F	MX-2202	QQF40032TT
M14	Hi-speed C-MOS, FF TC40H175F	MX-2206	QQF40175TT
M15	Hi-speed C-MOS, Buffer TC40H367F	MX-2208	QQF40367TT
M16	Hi-speed C-MOS, Decoder TC40H138F	MX-2203	QQF40138TT
M17	Hi-speed C-MOS, NAND TC40H000F	MX-2201	QQF40000TT
M18	Hi-speed C-MOS, Timer D1990AC	AMX-5801	QQ001990BA
M19	C-MOS, CPU MSM80C85ARS	AMX-5806	QQ008085A5
M20,M21	Hi-speed C-MOS, Buffer TC40H367F	MX-2208	QQF40367TT
M22	C-MOS, UART D3-6402-9	AMX-5805	QQ006402AZ

Ref. No.	Description	RS Part No.	Mfr's Part No.
M23	Hi-speed C-MOS, Buffer	TC40H367F	MX-2208
M24	C-MOS, Schmitt Trigger	TC4584BF	MX-2200
M25	C-MOS, PIO	MSM81C55RS	MX-5577
M26	Hi-speed C-MOS, OR Gate	TC40H032F	MX-2202
M27	C-MOS, NAND Gate	TC4011BF	MX-2183
M28	C-MOS, Flip-Flop	TC4013BF	MX-2184
M29,M30	Bipolar, OP-Amp	TL064CN	AMX-5800
M31	C-MOS, MODEM	MC14412VP	AMX-5808
M32	Hi-speed C-MOS, Buffer	TC40H367F	MX-2208
M33	Hi-speed C-MOS, Selector	TC40H157F	MX-2205
M34,M35	C-MOS, Schmitt Trigger	TC4584BF	MX-2200
M36	C-MOS, Flip-Flop	TC4013BF	MX-2184
M37	Hi-speed C-MOS, NAND	TC40H000F	MX-2201
M38	Hi-speed C-MOS, NOR Gate	TC40H002F	
M39	Hi-speed C-MOS, Buffer	TC40H245F	MX-2207
M40	Hi-speed C-MOS, Buffer	TC40H244F	
M41,M42	Hi-speed C-MOS, Buffer	TC40H367F	MX-2208
M43	Hi-speed C-MOS, AND Gate	TC40H011F	

TRANSFORMERS

OT1	Transformer, MODEM	ATB-0472	TDZ19A002K
OT2	Transformer, Converter	ATA-0001	TCA9RZ0413

RESISTORS

R1	Chip	1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R2-R7	Chip	33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R8	Chip	1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R9	Not used			
R10-R12	Chip	1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R13	Metal Film	806ohm/1/4W/±1%	N-0577BEE	RQBXF8060X
R14	Chip	10k/1/8W/±5%	ND-281EBM	RJ8APJ103%
R15	Metal Film	33.2k/1/4W/±1%	N-0622BEE	RQBXF3322X
R16	Metal Film	2.05k/1/4W/±1%	N-0716BEE	RQBXF2051X
R17	Metal Film	73.2k/1/4W/±1%	N-0612BEE	RQBXF7322X
R18	Metal Film	590k/1/4W/±1%	N-0615BEE	RQBXF5903X
R19	Chip	15k/1/8W/±5%	ND-0297EBM	RJ8APJ153%
R20	Chip	470k/1/8W/±5%	ND-0423EBM	RJ8APJ474%
R21	Chip	620ohm/1/8W/±5%	ND-0181EBM	RJ8APJ621%
R22	Chip	390ohm/1/8W/±5%	ND-0162EBM	RJ8APJ391%
R23	Chip	10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R24	Metal Film	665ohm/1/4W/±1%	N-0765BEE	RQBXF6650X
R25	Metal Film	1.5k/1/4W/±1%	N-0206BEE	RQBXF1501X
R26	Chip	10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R27	Metal Film	1.3k/1/4W/±1%	N-0202BEE	RQBXF1301X
R28	Metal Film	3.3k/1/4W/±1%	N-0230BEE	RQBXF3301X
R29	Metal Film	280k/1/4W/±1%	N-0672BEE	RQBXF2803X
R30	Metal Film	422k/1/4W/±1%	N-0419BEE	RQBXF4223X
R31	Chip	2.2k/1/8W/±5%	ND-0216EBM	RJ8APJ222%
R32	Chip	22ohm/1/8W/±5%	ND-0078EBM	RJ8APJ220%
R33	Chip	10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R34	Chip	1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R35	Chip	10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R36	Chip	680ohm/1/8W/±5%	ND-0183EBM	RJ8APJ681%
R37	Chip	180k/1/8W/±5%	ND-0387EBM	RJ8APJ184%
R38	Metal Film	52.3k/1/4W/±1%	N-0613BEE	RQBXF5232X
R39	Chip	1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R40,R41	Chip	10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R42	Metal Film	2.3k/1/4W/±1%	N-0218BEE	RQBXF2301X

Ref. No.	Description	RS Part No.	Mfr's Part No.
R43	Metal Film 10k/1/4W/±1%	N-0281BEE	RQBXF1002X
R44	Metal Film 242k/1/4W/±1%	N-0558BEE	RQBXF2423X
R45	Metal Film 7.97k/1/4W/±1%	N-0769BEE	RQBXF7971X
R46	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R47	Carbon 15M/1/4W/±5%	N-0486EEC	RD25PJ156X
R48	Chip 68k/1/8W/±5%	ND-0354EBM	RJ8APJ683%
R49,R50	Chip 3.3k/1/8W/±5%	ND-0230EBM	RJ8APJ332%
R51	Chip 2.2k/1/8W/±5%	ND-0216EBM	RJ8APJ222%
R52	Chip 1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R53	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R54	Chip 12k/1/8W/±5%	ND-0288EBM	RJ8APJ123%
R55	Chip 3.3k/1/8W/±5%	ND-0230EBM	RJ8APJ332%
R56	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R57	Not used		
R58-R62	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R63	Chip 620ohm/1/8W/±5%	ND-0181EBM	RJ8APJ621%
R64-R66	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R67	Not used		
R68	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R69	Not used		
R70-R74	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R75	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R76,R77	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R78	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R79,R80	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R81	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R82	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R83	Chip 22k/1/8W/±5%	ND-0311EBM	RJ8APJ223%
R84	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R85	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R86	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R87-R89	Chip 6.2k/1/8W/±5%	ND-0260EBM	RJ8APJ622%
R90	Chip 15k/1/8W/±5%	ND-0297EBM	RJ8APJ153%
R91	Chip 330ohm/1/8W/±5%	ND-0159EBM	RJ8APJ331%
R92	Chip 18k/1/8W/±5%	ND-0303EBM	RJ8APJ183%
R93	Chip 68k/1/8W/±5%	ND-0354EBM	RJ8APJ683%
R94	Chip 330ohm/1/8W/±5%	ND-0159EBM	RJ8APJ331%
R95	Chip 100ohm/1/8W/±5%	ND-0132EBM	RJ8APJ101%
R96	Chip 18k/1/8W/±5%	ND-0303EBM	RJ8APJ183%
R97	Chip 180ohm/1/8W/±5%	ND-0144EBM	RJ8APJ181%
R98	Chip 18k/1/8W/±5%	ND-0303EBM	RJ8APJ183%
R99	Chip 330ohm/1/8W/±5%	ND-0159EBM	RJ8APJ331%
R100	Not used		
R101	Chip 1.8k/1/8W/±5%	ND-0210EBM	RJ8APJ182%
R102	Chip 82k/1/8W/±5%	ND-0360EBM	RJ8APJ823%
R103	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R104	Chip 56k/1/8W/±5%	ND-0345EBM	RJ8APJ563%
R105	Metal Film 2.7k/1/4W/±1%	N-0224BEE	RQBXF2701X
R106	Chip 150k/1/8W/±5%	ND-0384EBM	RJ8APJ154%
R107	Chip 47k/1/4W/±5%	ND-0340EBM	RJ8APJ473%
R108	Metal Film 22.6k/1/4W/±1%	N-0729BEE	RQBXF2262X
R109	Chip 56k/1/8W/±5%	ND-0345EBM	RJ8APJ563%
R110,R111	Chip 150k/1/8W/±5%	ND-0384EBM	RJ8APJ154%
R112	Chip 1.8k/1/8W/±5%	ND-0210EBM	RJ8APJ182%
R113	Chip 3.3k/1/8W/±5%	ND-0230EBM	RJ8APJ332%
R114	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R115	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R116	Metal Film 150k/1/4W/±1%	N-0384BEE	RQBXF1503X

Ref. No.	Description	RS Part No.	Mfr's Part No.
R117,R118	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R119	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R120	Chip 82k/1/8W/±5%	ND-0360EBM	RJ8APJ823%
R121	Chip 820ohm/1/8W/±5%	ND-0187EBM	RJ8APJ821%
R122	Chip 470ohm/1/8W/±5%	ND-0169EBM	RJ8APJ471%
R123	Chip 1.8k/1/8W/±5%	ND-0210EBM	RJ8APJ182%
R124,R125	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R126	Chip 270ohm/1/8W/±5%	ND-0155EBM	RJ8APJ271%
R127	Chip 22k/1/8W/±5%	ND-0311EBM	RJ8APJ223%
R128	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R129-R130	Not used		
R131	Chip 1k/1/8W/±5%	ND-0196EBM	RJ8APJ102%
R132	Chip 150k/1/8W/±5%	ND-0384EBM	RJ8APJ154%
R133	Not used		
R134	Chip 3.3k/1/8W/±5%	ND-0230EBM	RJ8APJ332%
R135,R136	Chip 68k/1/8W/±5%	ND-0354EBM	RJ8APJ683%
R137-R139	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R140	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R141	Chip 1M/1/8W/±5%	ND-0445EBM	RJ8APJ105%
R142	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R143	Not used		
R144,R145	Chip 15k/1/8W/±5%	ND-0297EBM	RJ8APJ153%
R146	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R147,R148	Not used		
R149	Chip 56k/1/8W/±5%	ND-0345EBM	RJ8APJ563%
R150	Chip 470ohm/1/8W/±5%	ND-0169EBM	RJ8APJ471%
R151	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R152	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R153	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R154	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R155	Not used		
R156	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R157	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R158-R160	Chip 100k/1/8W/±5%	ND-0371EBM	RJ8APJ104%
R161	Chip 10k/1/8W/±5%	ND-0281EBM	RJ8APJ103%
R162	Chip 100ohm/1/8W/±5%	ND-0132EBM	RJ8APJ101%
R163-R170	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
R171	Cement 39 ohm/3W		RF03SJ390B
R172	Chip 33k/1/8W/±5%	ND-0324EBM	RJ8APJ333%
RESISTOR ARRAYS			
MR1,MR2	Not used		
MR3	Resistor, Array 33kX8/1/8W/±20%	ARX-0345	RAB333M08X
MR4	Not used		
MR5	Resistor, Array 100kX8/1/8W/±20%	ARX-0344	RAB104M08X
RELAYS			
RY1	FBR211CD005-M	AR-8160	ZRA265101Z
RY2	FRL-764D05/1AS-T	AR-8159	ZRA164102Z
RY3	MZ-5HS-FC	AR-8001	ZRA161301Z
SWITCHES			
SW1	Slide, SLD-22-456	AS-0004	SS020270ZZ
SW2	Slide, ST-011-01	AS-0006	SS040217ZZ
SW3	Slide, SLBT22BP-07	AS-0005	SS020271ZL
SW4	Push, SPJ 312U, without Knob	AS-7573	SP01ABA06A
SW5	Slide, SLD-22-456	AS-0004	SS020270ZZ

Ref. No.	Description	RS Part No.	Mfr's Part No.
TRANSISTORS			
T1	Silicon, 2SA1162, PNP, SY or SG	MX-6469	QUA1162XDP
T2-T7	Silicon, 2SC3052, NPN, No-Rank	2SC-2712Y	QUC3052XCP
T8	Not used		
T9-T11	Silicon, 2SC3052, NPN, No-Rank	2SC-2712Y	QUC3052XCP
T12	Not used		
T13-T17	Silicon, 2SC2712, NPN, LG	2SC-2712	QUC2712XCP
T18	Silicon, 2SC3052, NPN, No-Rank	2SC-2712Y	QUC3052XCP
T19	Silicon, 2SA1162, PNP, SY or SG	MX-6469	QUA1162XDP
T20	Silicon, 2SC3052, NPN, No-Rank	2SC-2712Y	QUC3052XCP
T21	Silicon, 2SC1384, NPN, S-Rank	2SC-1384	QTC1384XHN
T22	Silicon, 2SC2712, NPN, LG	2SC-2712	QUC2712XCP
T23-T25	Silicon, 2SC3052, NPN, No-Rank	2SC-2712Y	QUC3052XCP
T26	Not used		
T27	Silicon, 2SC3052, NPN, No-Rank	2SC-2712Y	QUC3052XCP
T28	Silicon, 2SA1162, PNP, SY or SG	MX-6469	QUA1162XDP
THERMISTORS			
TH1,TH2	10k ohm/±5%, TD5-C310D1H	AT-1235	QHQC31HZP
VARIABLE RESISTORS			
VR1	50k B-curve, Contrast	AP-7424	RPSNB50306
VR2	Semi-fixed, 50k B-curve, MODEM	AP-7336	RPSNB50303
CRYSTAL OSCILLATORS			
X1	32.768 kHz for Clock	MX-2170	XTR1A1001%
X2	4.9152 MHz for CPU Clock	AMX-1010	XBR1A1003X
X3	HC43U/1MHz for Modem	AMX-1009	XAZ1C2001X

LCD PCB Assembly

Ref. No.	Description	RS Part No.	Mfr's Part No.
CAPACITORS			
C1-C4	Ceramic	0.1 μ F/25V/+80-20%	CD-104ZFPC CFPC104ZF%
C5	Ceramic	18pF/25V/ \pm 10%	CD-180KFCX CFTC180KC%
C6-C10	Ceramic	0.1 μ F 25V/+80-20%	CD-104ZFPC CFPC104ZF%
C11-C20	Ceramic	1000pF/25V/+80-20%	CD-102ZFCX CFPC102ZF%
CONNECTOR			
CN1	Jack, Junction to Main PCB		YJF30S012Z
INTEGRATED CIRCUITS			
M1-M5	C-MOS Driver	HD44102CRH	MX-2169 QQ044102CB
M6-M10	C-MOS Driver	HD44102CH	AMX-5797 QQ044102BB
M11,M12	C-MOS Driver	HD44103BLD	AMX-5798 QQ044103BB
M13	C-MOS OP-Amp	LA6324	AMX-5796 QQF06324AC
LED			
LED	SLP-135B	AL-1458	QL1SP135BC
RESISTORS			
R1,R2	Chip	10k ohm/1/8W \pm 2%	ND-0281CBM RJ8APG103%
R3	Chip	26.5k ohm/1/8W \pm 2%	ND-0271CBM RJ8APGA52%
R4,R5	Chip	10k ohm/1/8W \pm 2%	ND-0281CBM RJ8APG103%
R6-R10	Chip	100k ohm/1/8W \pm 5%	ND-0371EBM RJ8APJ104%
R11	Chip	18 ohm/1/8W \pm 5%	ND-0144EBM RJ8APJ180%
R12-R16	Chip	150 ohm/1/8W \pm 5%	ND-0142EBM RJ8APJ151%

Keyboard Assembly

Ref. No.	Description	RS Part No.	Mfr's Part No.
1-1	Keyboard Kit		AGX1000*02
1-1-1	Spring - SPACE Key	ARB-7737	MW261LJ019
1-1-2	Guide - ENTER Key	AHC-3111	MX422LJ003
1-1-3	Guide - SPACE Key	AHC-3112	MX722LJ002
1-1-4	Lever Guide - ENTER and SPACE Key	AHC-3113	VK112SB001
1-1-5	Lever Stopper - ENTER and SPACE Key	AHC-3114	VK113SH001
1-1-6	Key Guide Pin - SPACE Key	AHC-3115	VM253SH001
1-1-7	Key Guide - SPACE Key	AHC-3116	VM276SB001
1-2	Keytop Kit		AG102***02
1-2-1	Keytop - TACT	AK-5651	VK121SB007
1-2-2	Keytop - 1	AK-5206	VK122SB004
1-2-3	Keytop - 2	AK-5207	VK122SB005
1-2-4	Keytop - 3	AK-5208	VK122SB006
1-2-5	Keytop - 4	AK-5209	VK122SB007
1-2-6	Keytop - 5	AK-5210	VK122SB008
1-2-7	Keytop - 6	AK-5211	VK122SB009
1-2-8	Keytop - 7	AK-5212	VK122SB010
1-2-9	Keytop - 8	AK-5213	VK122SB011
1-2-10	Keytop - 9	AK-5214	VK122SB012
1-2-11	Keytop - 0	AK-5215	VK122SB013
1-2-12	Keytop - A	AK-5216	VK122SB014
1-2-13	Keytop - B	AK-5217	VK122SB015
1-2-14	Keytop - C	AK-5218	VK122SB016
1-2-15	Keytop - D	AK-5219	VK122SB017
1-2-16	Keytop - E	AK-5220	VK122SB018
1-2-17	Keytop - F	AK-5221	VK122SB019
1-2-18	Keytop - G	AK-5222	VK122SB020
1-2-19	Keytop - H	AK-5223	VK122SB021
1-2-20	Keytop - I	AK-5224	VK122SB022
1-2-21	Keytop - J	AK-5225	VK122SB023
1-2-22	Keytop - G	AK-5226	VK122SB024
1-2-23	Keytop - L	AK-5227	VK122SB025
1-2-24	Keytop - M	AK-5228	VK122SB026
1-2-25	Keytop - N	AK-5229	VK122SB027
1-2-26	Keytop - O	AK-5230	VK122SB028
1-2-27	Keytop - P	AK-5231	VK122SB029
1-2-28	Keytop - Q	AK-5232	VK122SB030
1-2-29	Keytop - R	AK-5233	VK122SB031
1-2-30	Keytop - S	AK-5234	VK122SB032
1-2-31	Keytop - T	AK-5235	VK122SB033
1-2-32	Keytop - U	AK-5236	VK122SB034
1-2-33	Keytop - V	AK-5237	VK122SB035
1-2-34	Keytop - W	AK-5238	VK122SB036
1-2-35	Keytop - X	AK-5239	VK122SB037
1-2-36	Keytop - Y	AK-5240	VK122SB038
1-2-37	Keytop - Z	AK-5241	VK122SB039
1-2-38	Keytop - ESC	AK-5242	VK122SB040
1-2-39	Keytop - MINUS	AK-5243	VK122SB041
1-2-40	Keytop - PLUS	AK-5244	VK122SB042
1-2-41	Keytop - DEL	AK-5245	VK122SB043
1-2-42	Keytop - BRACKET	AK-5246	VK122SB044
1-2-43	Keytop - ;	AK-5247	VK122SB045
1-2-44	Keytop - QUOTATION	AK-5248	VK122SB046
1-2-45	Keytop - CAPSL	AK-5249	VK122SB047
1-2-46	Keytop - COMMA	AK-5250	VK122SB048
1-2-47	Keytop - PERIOD	AK-5251	VK122SB049
1-2-48	Keytop - /	AK-5252	VK122SB050
1-2-49	Keytop - GRPH	AK-5253	VK122SB051

Ref. No.	Description	RS Part No.	Mfr's Part No.
1-2-50	Keytop - CODE	AK-5254	VK122SB052
1-2-51	Keytop - NUM	AK-5255	VK122SB053
1-2-52	Keytop - TAB	AK-5256	VK132SB006
1-2-53	Keytop - CTRL	AK-5257	VK132SB007
1-2-54	Keytop - SHIFT	AK-5654	VK132SB008
1-2-55	Keytop - ENTER	AK-5655	VK142SB003
1-2-56	Keytop - SPACE	AK-5261	VK172SB002
1-3	Diode, Silicon, 1S2076	ADX-1763	QDSS2076#B
1-4	Switch, Key - Tact	AS-2910	SK0101X22T
1-5	Switch, Key - Lock	AS-2886	SK0111X08A
1-6	Switch, Key - Push	AS-2911	SK0111X12A
1-7	Insulator		VS873YB001
1-8	Cushion		VS875YB002
1-9	Jack, Junction to Main PCB	AJ-0010	YJF18S016Z

Mechanical and Assembly Parts List

Ref. No.	Description	RS Part No.	Mfr's Part No.
1	Keyboard Assembly	AXX-0238	AFY102***1
2	LCD PCB Assembly	AX-4001	APLX142AAQ
2-1	Frame, LCD		MB861SF002
2-3	Connector, LCD SG type	AJ-7321	VQ811RX001
2-5	LCD, LR202-C	AL1459	ZXLR202CXB
3	Main PCB Assembly	AX-4002	APLX144AAQ
3-1	Case Assembly, Battery	AZ-0010	AM102***03
3-1-1	Battery Terminal, Plus		MW161SN001
3-1-2	Battery Terminal, Minus		MW161SN002
3-1-3	Battery Terminal, Rear		MW261LJ009
3-1-4	Battery Terminal, Front		MW261LJ010
3-1-5	Case, Battery, Black		VB662SB003
3-2	Knob, Contrast, Black	AK-5657	VF187SB003
3-3	Knob, RESET, Black	AK-5265	VK121SB004
3-4	Flat Cable, For Keyboard, 18 Lines	AW-0006	WC18140AD1
3-5	Flat Cable, For LCD, 30 Lines	AW-0007	WC30150BD1
3-6	IC Socket, 28-pin, DICF-28CS	AJ-7349	YSC28S005Z
3-7	IC Socket, 28-pin, 5500-28A	AJ-7637	YSC28S007Z
3-8	Battery, Nickel-Cadmium, 3-51FT	ACS-0100	ZBN036102Y
3-9	Buzzer, KBS-27DB-3T		ZYED100068
4	Case Assembly, Top, Ivory	AZ-0011	AM102***01
4-1	Case, Top, Ivory		VB883SH004
4-2	Filter		VS868AC005
4-3	Plate, Model		VVM102***2
5	Case Assembly, Bottom, Black	AZ-0012	AM102***02
5-1	Foot, Rubber		##P4157***
5-2	Case, Bottom, Black		VB883SB012
6	Screw, Cup Head, Sems, Machine, M3X8, S-ZNCR	AHD-1865	BSP43008NZ
7	Plate, Name		KLX1***01
8	Label, FCC (USA Version Only)		KL000355XX
9	Plate, Serial Number		MVS102***1
10	Cap, BCR Connector Cover	AHC-2235	VE32JPB001
11	Cover, Knob	AHC-0012	VN230SB007
12	Cover, ROM	AHC-0013	VS667SB004
13	Cover, Battery	AHC-0014	VS668SB004
14	Cap, Printer Connector Cover	ART-5559	VU521SB001
15	Cap, System Bus Connector Cover	AHC-0016	VU611SB001
16	Plate, Fiber		VS875FB003
17	Nut, M2.6, Thin Type, S-ZNCR		BNHCL26NSZ
18	Screw, Pan Head, Machine, M3X8, S-ZNCR		BSPC3008NZ
19	Screw, Pan Head, Machine, M2.6X12, S-ZNCR		BSPF2612NZ
20	Screw, Cup Head, Machine, M1.7X3, S-BLACK		BSP21703NB
21	Screw, Pan Head, Tapping, M3X8, S-ZNCR		BTTP3008PZ
	Hardware Kit	AHW-	AYXM102*01
	4 Screws, Pan Head, Tapping, M3X10, S-ZNCR	2603803	
	Pouch	AZ-0013	AM102***04

VII. SCHEMATIC DIAGRAMS/PCB VIEWS

Schematic Diagrams

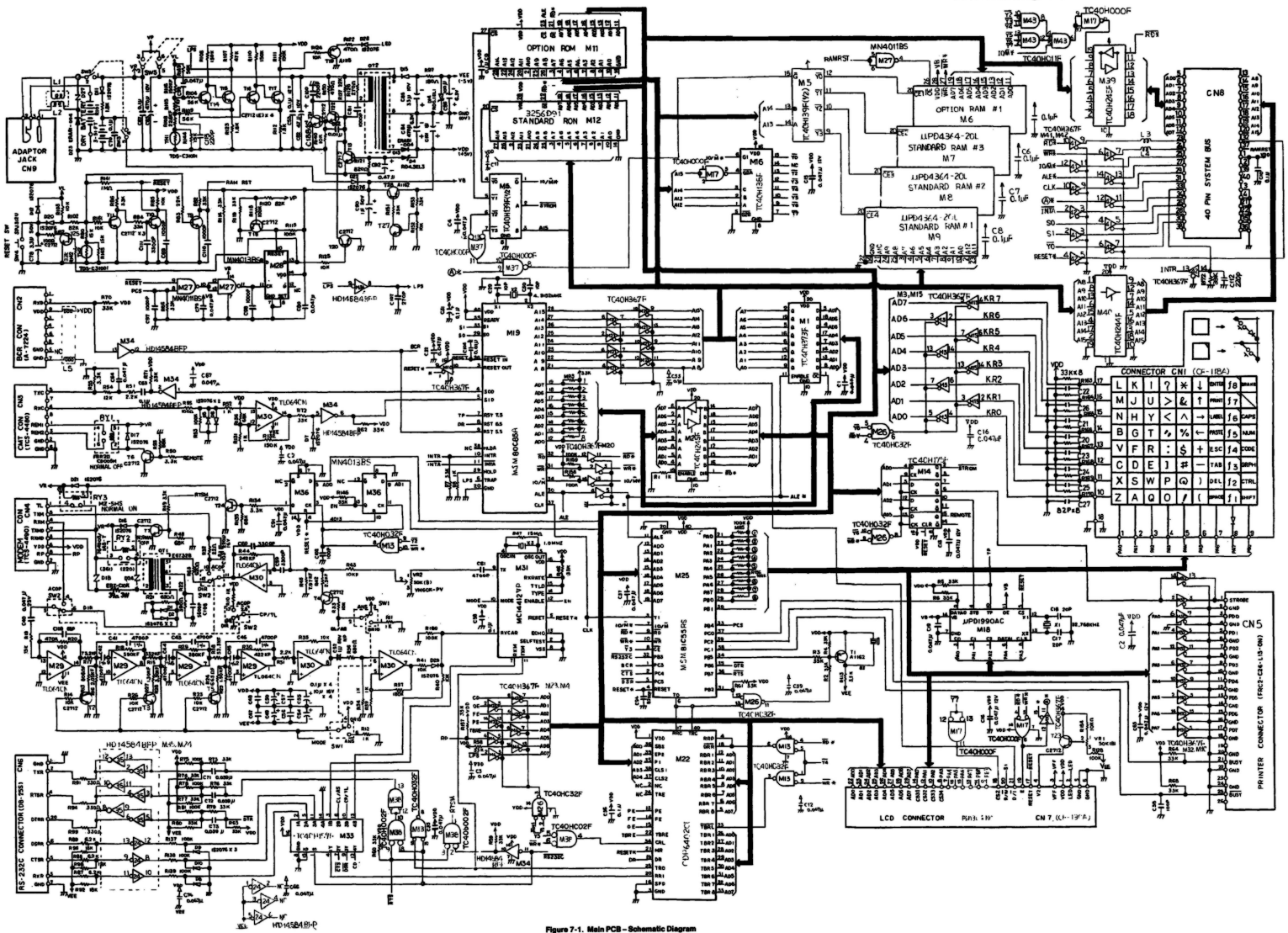


Figure 7-1. Main PCB - Schematic Diagram

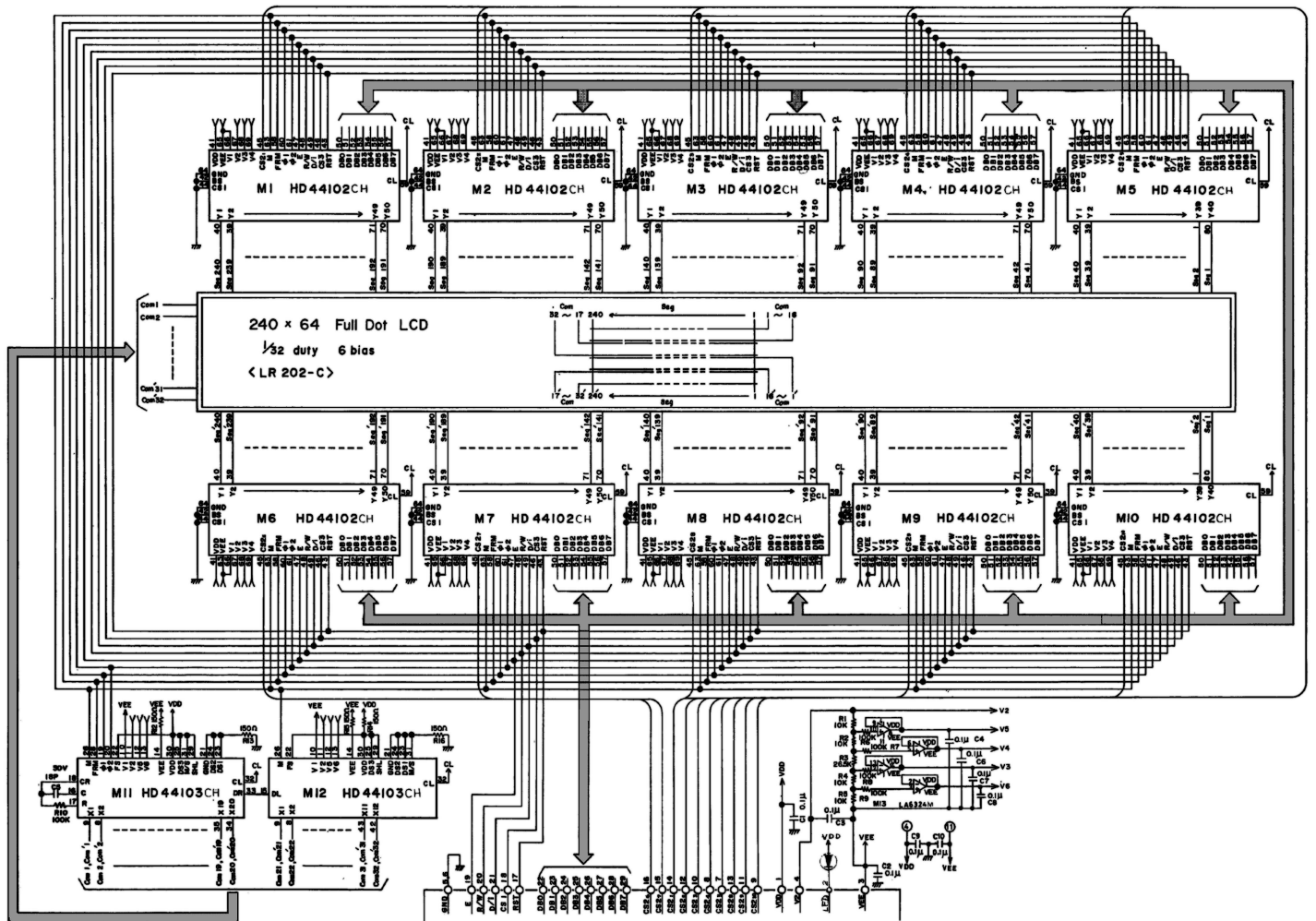


Figure 7-2. LCD PCB – Schematic Diagram

[illegible]

7-3

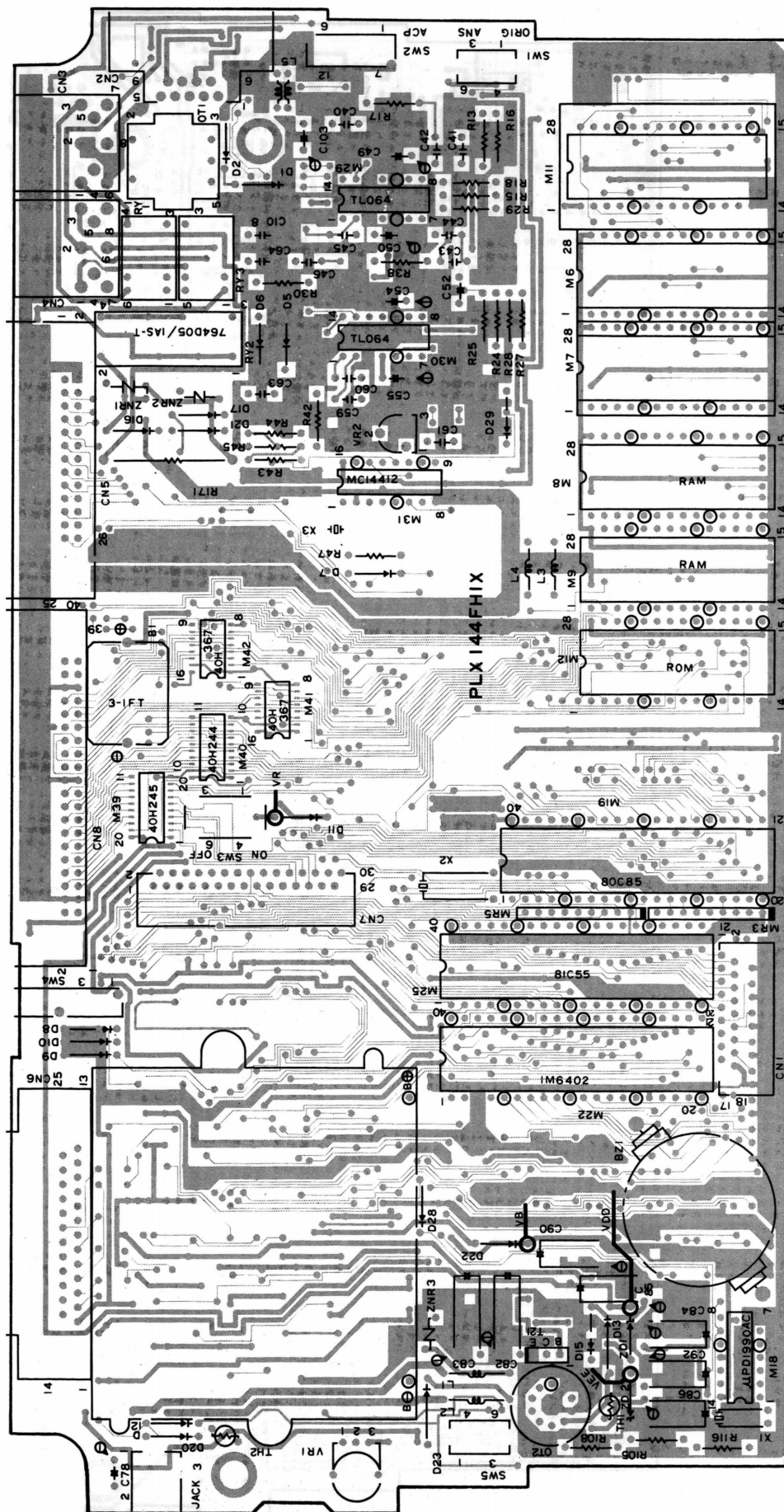


Figure 7-4. Main PCB - Bottom View

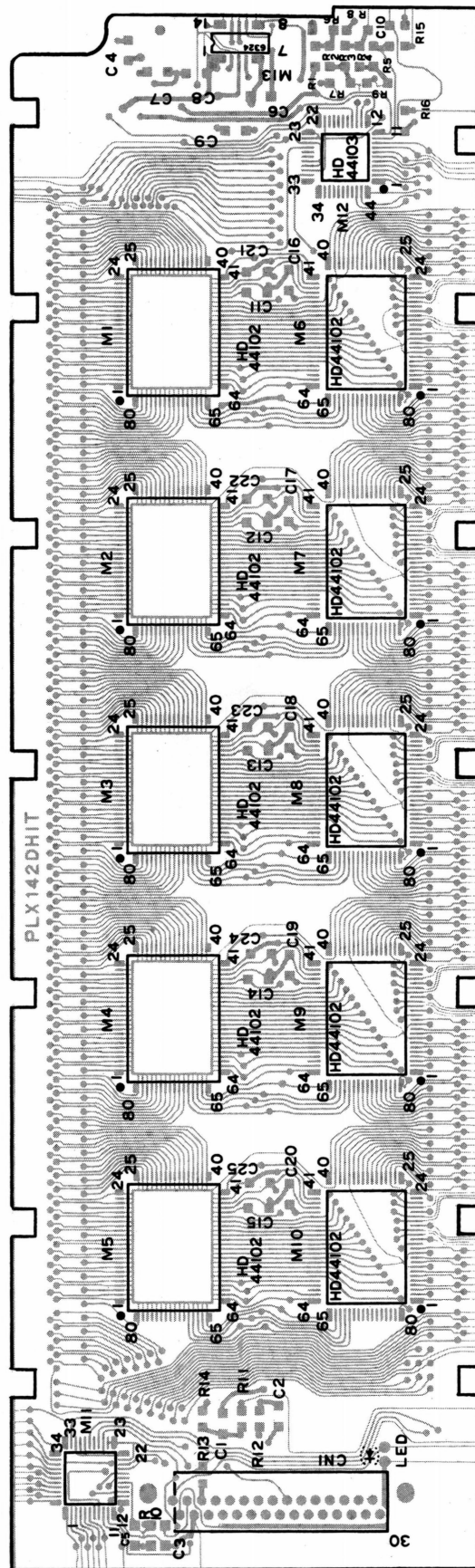


Figure 7-5. LCD PCB – Top View

APPENDIX A /INSTALLATION

Installation of Optional RAM and ROM

- Using a coin, remove the RAM and ROM cover on the bottom case.
- Insert the optional RAM into the IC socket marked M6.
- Insert the optional ROM into the IC socket marked M11.

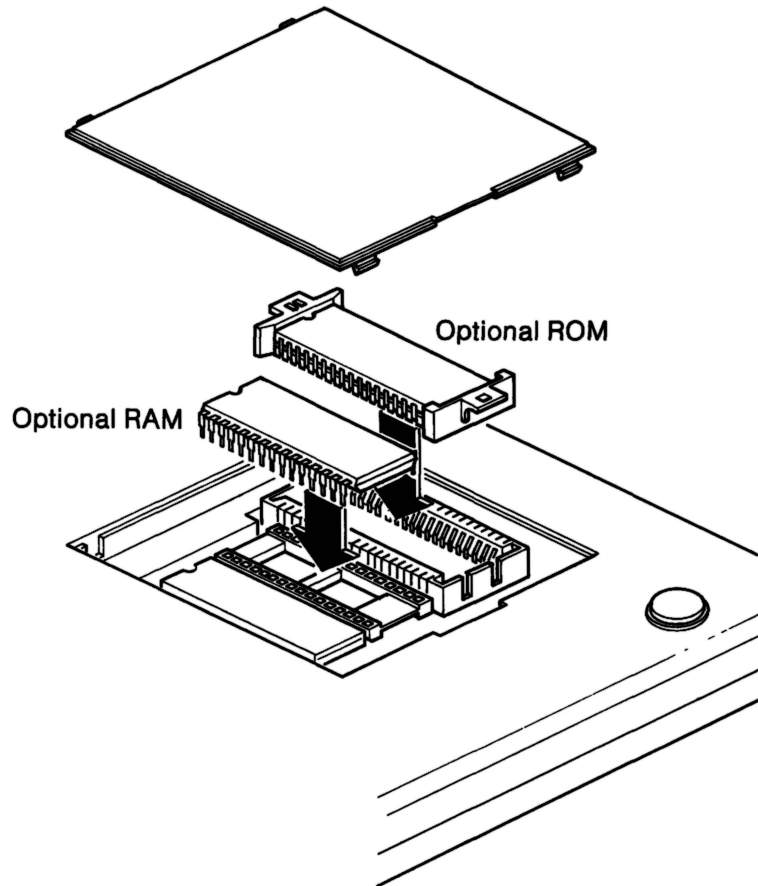


Figure A-1. Installation of RAM and ROM

APPENDIX B/KEYBOARD LAYOUT,
CONNECTOR PIN ASSIGNMENTS AND
CHARACTER CODE TABLE

B-1. Keyboard Layout

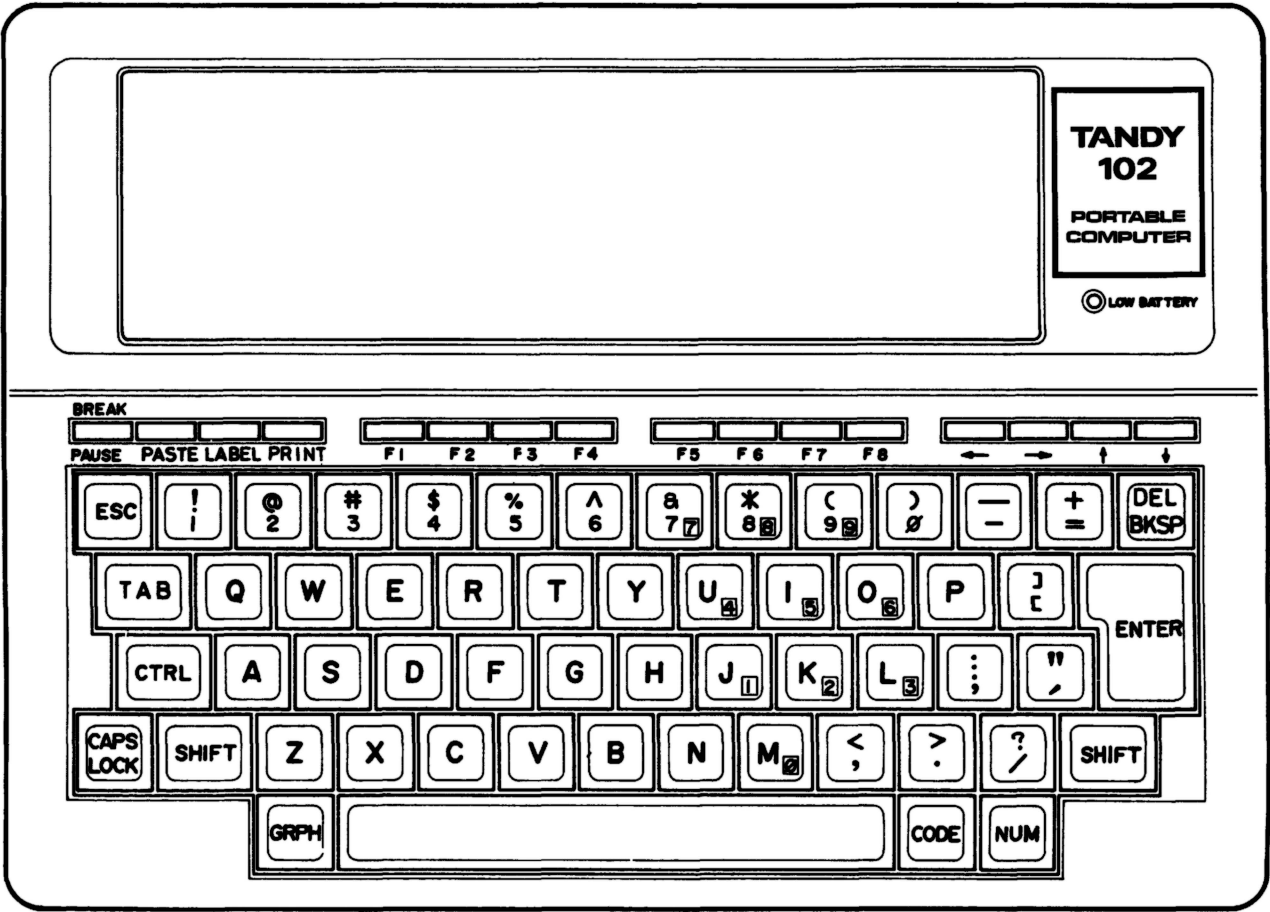


Figure B-1. Keyboard Layout

B-2. Connector Pin Assignments

B-2-1. System Bus Interface

Pin No.	Symbol	Description
1	VDD	
2	VDD	
3	GND	
4	GND	
5	D0	Address and data signal bit 0
6	D1	Address and data signal bit 1
7	D2	Address and data signal bit 2
8	D3	Address and data signal bit 3
9	D4	Address and data signal bit 4
10	D5	Address and data signal bit 5
11	D6	Address and data signal bit 6
12	D7	Address and data signal bit 7
13	A8	Address signal bit 8
14	A9	Address signal bit 9
15	A10	Address signal bit 10
16	A11	Address signal bit 11
17	A12	Address signal bit 12
18	A13	Address signal bit 13
19	A14	Address signal bit 14
20	A15	Address signal bit 15
21	GND	
22	GND	
23	\overline{RD}	Read enable signal
24	\overline{WR}	Write enable signal
25	$\overline{IO/\overline{M}}$	I/O or memory select signal
26	SO	Status 0 signal
27	ALE	Address latch enable signal
28	S1	Status 1 signal
29	CLK	CLock signal
30	\overline{IOCONT}	I/O controller select signal
31	E	I/O or memory access enable signal
32	RESET	Reset signal
33	\overline{INTR}	Interrupt request signal
34	\overline{INTA}	Interrupt acknowledge signal
35	GND	
36	GND	
37	\overline{RAMRST}	RAM enable signal
38	NC	
39	NC	
40	NC	

Table B-1. System Bus Connector Pin Assignments

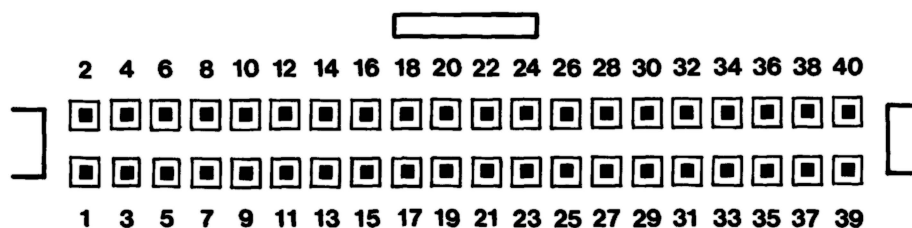


Figure B-2. System Bus Connector

B-2-2. RS-232C Interface

Pin No.	Symbol	Description
1	GND	
2	TXR	Transmit Data
3	RXR	Receive Data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7	GND	
8	CD	Carrier detect
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	DTR	Data terminal ready
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	

Table B-2. RS-233C Connector Pin Assignments

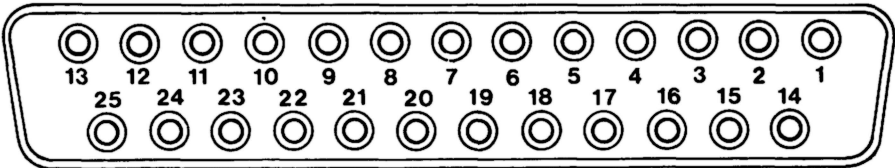


Figure B-3. RS-232C Connector

B-2-3. Printer Interface

Pin No.	Symbol	Description
1	<u>STROBE</u>	STROBE Pulse
2	GND	
3	PD0	Bit 0 of Print Data
4	GND	
5	PD1	Bit 1 of Print Data
6	GND	
7	PD2	Bit 2 of Print Data
8	GND	
9	PD3	Bit 3 of Print Data
10	GND	
11	PD4	Bit 4 of Print Data
12	GND	
13	PD5	Bit 5 of Print Data
14	GND	
15	PD6	Bit 6 of Print Data
16	GND	
17	PD7	Bit 7 of Print Data
18	GND	
19	NC	
20	GND	
21	BUSY	Busy Signal for Computer
22	GND	
23	NC	
24	GND	
25	<u>BUSY</u>	Select Signal
26	NC	

Table B-3. Printer Connector Pin Assignments

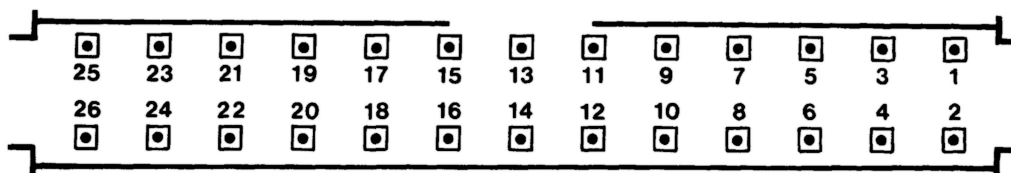


Figure B-4. Printer Connector

B-2-4. Cassette Interface

Pin No.	Symbol	Description
1	REM 1	Remote Remote Receive data for CMT Transmit data for CMT
2	GND	
3	REM 2	
4	R × C	
5	T × C	
6	GND	
7	NC	
8	NC	

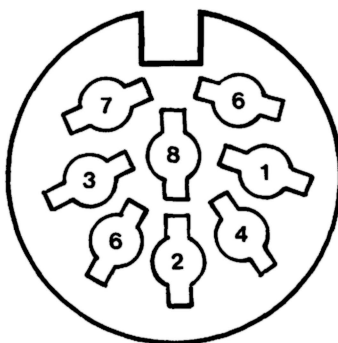


Figure B-5. Cassette Connector

B-2-5. MODEM Interface

Pin No.	Symbol	Description
1	TL	Conventional Telephone Unit
2	GND	
3	R × MD	
4	R × MC	Direct Connection to Tel Line (RING)
5	T × MC	Acoustic Coupler Connection (MIC)
6	VDD	Acoustic Coupler Connection (Speaker)
7	T × MD	Direct Connection to Tel Line (TIP)
8	RP	Ringing Pulse

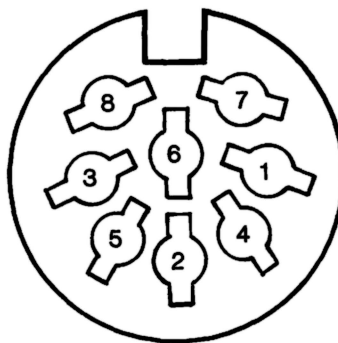


Figure B-6. MODEM Connector

B-2-6. Bar Code Reader Interface

Pin No.	Symbol	Description
1	NC	Receive data from bar code reader
2	R × DB	
3	NC	
4	NC	
5	NC	
6	NC	
7	GND	
8	NC	
9	VDD	

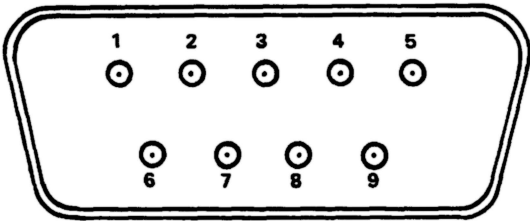




Figure B-7. Bar Code Reader Connector

B-3. Character Code Table

Decimal	Hex	Binary	Displayed Character	Keyboard Character
00	00	00000000		CTRL @
1	01	00000001		CTRL A
2	02	00000010		CTRL B
3	03	00000011		CTRL C
4	04	00000100		CTRL D
5	05	00000101		CTRL E
6	06	00000110		CTRL F
7	07	00000111		CTRL G
8	08	00001000		CTRL H
9	09	00001001		CTRL I
10	0A	00001010		CTRL J
11	0B	00001011		CTRL K
12	0C	00001100		CTRL L
13	0D	00001101		CTRL M
14	0E	00001110		CTRL N
15	0F	00001111		CTRL O
16	10	00010000		CTRL P
17	11	00010001		CTRL Q
18	12	00010010		CTRL R
19	13	00010011		CTRL S
20	14	00010100		CTRL T
21	15	00010101		CTRL U
22	16	00010110		CTRL V
23	17	00010111		CTRL W
24	18	00011000		CTRL X


























25	19	00011001		CTRL Y
26	1A	00011010		CTRL Z
27	1B	00011011		ESC
28	1C	00011100		→
29	1D	00011101		←
30	1E	00011110		↑
31	1F	00011111		↓
32	20	00100000		SPACEBAR
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#
36	24	00100100	\$	\$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	((
41	29	00101001))
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	-	-
46	2E	00101110	.	.
47	2F	00101111	/	/
48	30	00110000	0	0
49	31	00110001	1	1


























Decimal	Hex	Binary	Displayed Character	Keyboard Character
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J

Decimal	Hex	Binary	Display Character	Keyboard Character
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[[
92	5C	01011100	\	 -
93	5D	01011101]]
94	5E	01011110	^	^
95	5F	01011111	_	_
96	60	01100000	`	 [
97	61	01100001	a	a
98	62	01100010	b	b
99	63	01100011	c	c

Decimal	Hex	Binary	Displayed Character	Keyboard Character
100	64	01100100	d	d
101	65	01100101	e	e
102	66	01100110	f	f
103	67	01100111	g	g
104	68	01101000	h	h
105	69	01101001	i	i
106	6A	01101010	j	j
107	6B	01101011	k	k
108	6C	01101100	l	l
109	6D	01101101	m	m
110	6E	01101110	n	n
111	6F	01101111	o	o
112	70	01110000	p	p
113	71	01110001	q	q
114	72	01110010	r	r
115	73	01110011	s	s
116	74	01110100	t	t
117	75	01110101	u	u
118	76	01110110	v	v
119	77	01110111	w	w
120	78	01111000	x	x
121	79	01111001	y	y
122	7A	01111010	z	z
123	7B	01111011	{	[9
124	7C	01111100		[_












Decimal	Hex	Binary	Displayed Character	Keyboard Character
125	7D	01111101	}	[0
126	7E	01111110	~	[]
127	7F	01111111		[DEL
128	80	10000000	⌘	[CMD p
129	81	10000001	⌘	[CMD m
130	82	10000010	⌘	[CMD f
131	83	10000011	⌘	[CMD x
132	84	10000100	⌘	[CMD c
133	85	10000101	⌘	[CMD a
134	86	10000110	⌘	[CMD h
135	87	10000111	⌘	[CMD t
136	88	10001000	⌘	[CMD l
137	89	10001001	⌘	[CMD r
138	8A	10001010	⌘	[CMD /
139	8B	10001011	⌘	[CMD s
140	8C	10001100	⌘	[CMD ']
141	8D	10001101	⌘	[CMD =
142	8E	10001110	⌘	[CMD i
143	8F	10001111	⌘	[CMD e
144	90	10010000	⌘	[CMD y-
145	91	10010001	⌘	[CMD u
146	92	10010010	⌘	[CMD ;
147	93	10010011	⌘	[CMD q
148	94	10010100	⌘	[CMD w
149	95	10010101	⌘	[CMD b

Decimal	Hex	Binary	Displayed Character	Keyboard Character
150	96	10010110	¶	 n
151	97	10010111	⌘	 .
152	98	10011000	↑	 o
153	99	10011001	↓	 ,
154	9A	10011010	→	 l
155	9B	10011011	←	 k
156	9C	10011100	⌕	 2
157	9D	10011101	⌕	 3
158	9E	10011110	♥	 4
159	9F	10011111	♣	 5
160	A0	10100000	'	 ' ,
161	A1	10100001	à	 z
162	A2	10100010	ç	 f
163	A3	10100011	£	 8
164	A4	10100100	`	 " ' ,
165	A5	10100101	µ	]
166	A6	10100110	÷	)
167	A7	10100111	¶	 _
168	A8	10101000	†	 +
169	A9	10101001	§	 s
170	AA	10101010	¶	 R
171	AB	10101011	¶	 Y
172	AC	10101100	¼	 p
173	AD	10101101	¼	 ;
174	AE	10101110	½	 /

Decimal	Hex	Binary	Displayed Character	Keyboard Character
175	AF	10101111	¶	 0
176	B0	10110000	¥	 7
177	B1	10110001	À	 Q
178	B2	10110010	Ö	 O
179	B3	10110011	Û	 U
180	B4	10110100	☼	 6
181	B5	10110101	˜	 [
182	B6	10110110	ä	 q
183	B7	10110111	ö	 o
184	B8	10111000	ü	 u
185	B9	10111001	ß	 S
186	BA	10111010	™	 T
187	BB	10111011	é	 d
188	BC	10111100	ù	 m
189	BD	10111101	è	 c
190	BE	10111110	..	 =
191	BF	10111111	ƒ	 F
192	C0	11000000	à	 1
193	C1	11000001	é	 3
194	C2	11000010	î	 8
195	C3	11000011	ó	 9
196	C4	11000100	û	 7
197	C5	11000101	^	 -
198	C6	11000110	ë	 e
199	C7	11000111	ï	 i

Decimal	Hex	Binary	Displayed Character	Keyboard Character
200	C8	11001000	À	a
201	C9	11001001	Á	k
202	CA	11001010	Â	l
203	CB	11001011	Ã	j
204	CC	11001100	ä	!
205	CD	11001101	Å	n
206	CE	11001110	æ	v
207	CF	11001111	ß	b
208	D0	11010000	À	X
209	D1	11010001	Á	x
210	D2	11010010	Â	W
211	D3	11010011	Ã	w
212	D4	11010100	Ä	>
213	D5	11010101	Å	.
214	D6	11010110	Ä	N
215	D7	11010111	É	D
216	D8	11011000	À	A
217	D9	11011001	á	K
218	DA	11011010	â	L
219	DB	11011011	ã	J
220	DC	11011100	ä	?
221	DD	11011101	å	M
222	DE	11011110	æ	C
223	DF	11011111	ä	Z
224	ED	11100000		Z

225	E1	11100001	■	!
226	E2	11100010	■	@
227	E3	11100011	■	#
228	E4	11100100	■	\$
229	E5	11100101	■	%
230	E6	11100110	■	^
231	E7	11100111	■	Q
232	E8	11101000	■	W
233	E9	11101001	■	E
234	EA	11101010	■	R
235	EB	11101011	■	A
236	EC	11101100	■	S
237	ED	11101101	■	D
238	EE	11101110	■	F
239	EF	11101111	■	X
240	F0	11110000	■	U
241	F1	11110001	■	P
242	F2	11110010	■	O
243	F3	11110011	■	I
244	F4	11110100	■	J
245	F5	11110101	■	:
246	F6	11110110	■	M
247	F7	11110111	■	>
248	F8	11111000	■	<
249	F9	11111001	■	L

Decimal	Hex	Binary	Displayed Character	Keyboard Character
250	FA	11111010	+	 K
251	FB	11111011		 H
252	FC	11111100		 T
253	FD	11111101		 G
254	FE	11111110		 Y
255	FF	11111111		 C

APPENDIX C/TECHNICAL INFORMATION

C-1. 80C85A

General Description

The 80C85A is a complete 8-bit, parallel central processor implemented in silicon gate C-MOS technology and compatible with 8085A.

It is designed with the same processing speed and lower power consumption compared with 8085A, thereby offering a high level of system integration.

The 80C85A uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

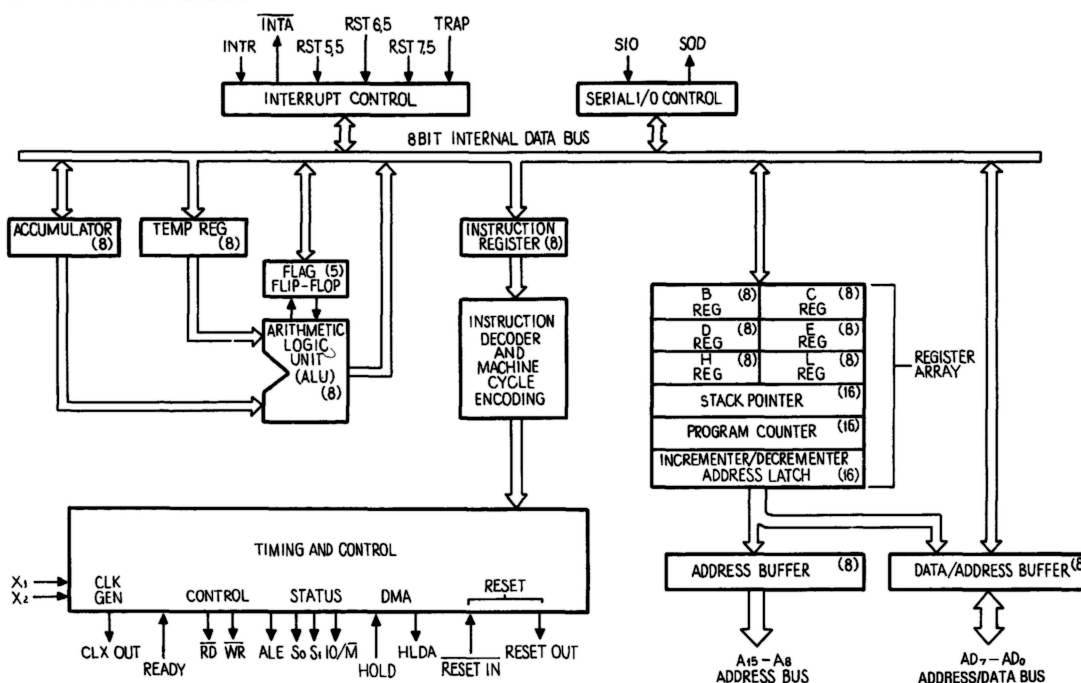


Figure C-1. Functional Block Diagram

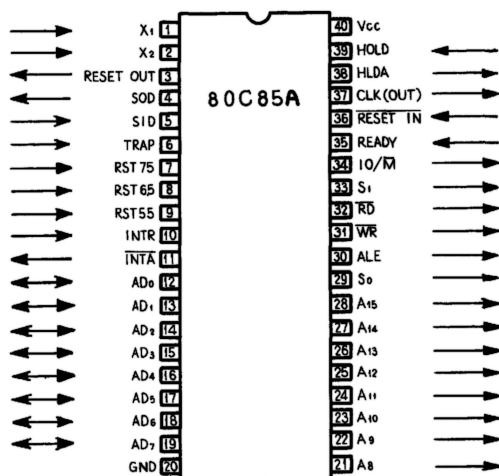


Figure C-2. Pin Configuration of 80C85A

Functional Pin Description

A₈ – A₁₅ (Output, 3-state)

Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD₀ – AD₇ (Input/Output, 3-state)

Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE (Output)

Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to be latched onto the on-chip latch of the peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

S₀, S₁ and IO/ \overline{M}

Machine cycle status:

IO/ \overline{M}	S ₁	S ₀	States	IO/ \overline{M}	S ₁	S ₀	States
0	0	1	Memory write	1	1	1	Interrupt Acknowledge
0	1	0	Memory read	.	0	0	Halt . = 3-state
1	0	1	I/O write	.	x	x	Hold (high impedance)
1	1	0	I/O read	.	x	x	Reset x = unspecified
0	1	1	Opcode fetch				

S₁ can be used as an advanced R/W status. IO/ \overline{M} , S₀ and S₁ become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

\overline{RD} (Output, 3-state)

READ control: A low level on \overline{RD} indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

\overline{WR} (Output, 3-state)

WRITE control: A low level on \overline{WR} indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of \overline{WR} , 3-stated during Hold and Halt modes and during RESET.

\overline{READY} (Input)

If \overline{READY} is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If \overline{READY} is low, the CPU will wait an integral number of clock cycles for \overline{READY} to go high before completing the read or write cycle. \overline{READY} must conform to specified setup and hold times.

HOLD (Input)

HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, \overline{RD} , \overline{WR} , and IO/ \overline{M} lines are 3-stated.

HLDA (Output)

HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.

INTR (Input)

INTERRUPT REQUEST: As a general purpose interrupt, it is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

 $\overline{\text{INTA}}$ (Output)

INTERRUPT ACKNOWLEDGE: Used instead of (and has the same timing as) $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted.

RST 5.5, RST 6.5, RST 7.5 (Input)

RESTART INTERRUPTS: These three inputs have the same timing as INTR, except that they cause an internal RESTART to be automatically inserted.

The priority of these interrupts is ordered as shown in Table C-1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

TRAP (Input)

Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5 – 7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table C-1.)

 $\overline{\text{RESET IN}}$ (Input)

Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.

RESET OUT (Output)

Indicates the CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.

 X_1, X_2 (Input)

X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.

CLK (Output)

Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (Output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

Vcc

+5 volt supply.

GND

Ground reference.

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched depends on the instruction provided to the CPU when the interrupt is acknowledged.

Table C-1. Interrupt Priority, Restart Address and Sensitivity

Function

The 80C85A has twelve addressable 8-bit registers. Four can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or a 16-bit register pair. The 80C85A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Register; data pointer (HL)	8-bit × 6 or 16-bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flag (8-bit space)

The 80C85A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle, the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle, the data bus is used for memory or I/O data.

The 80C85A provides RD, WR, S₀, S₁ and IO/M signals for bus control. An Interrupt Acknowledge signal (INTA) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The 80C85A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.

In addition to these features, 80C85A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The 80C85A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table C-1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 80C85A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP-highest priority, RST 7.5, RST 6.5, RST 5.5, INTR-lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure C-3 illustrates the TRAP interrupt request circuitry within the 80C85A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 – 7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

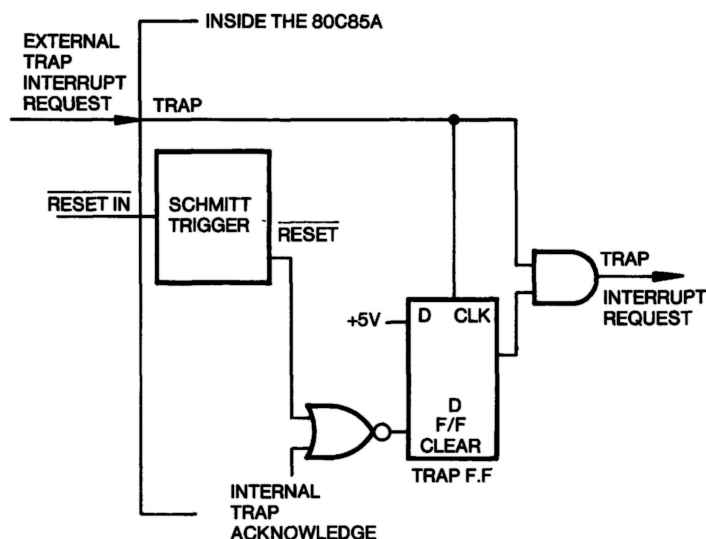


Figure C-3. Trap and RESET IN

Basic System Timing

The 80C85A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure C-4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($\overline{\text{IO/M}}$, S_1 , S_0) and the three control signals ($\overline{\text{RD}}$, $\overline{\text{WR}}$, and INTA). (See Table C-2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{\text{RD}}$ and $\overline{\text{WR}}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OP CODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be in one of ten possible states, shown in Table C-3.

Machine Cycle	Status			Control		
	$\overline{IO/\overline{M}}$	S_1	S_0	\overline{RD}	\overline{WR}	\overline{INTA}
Opcode Fetch (OF)	0	1	1	0	1	1
Memory Read (MR)	0	1	0	0	1	1
Memory Write (MW)	0	0	1	1	0	1
I/O Read (IOR)	1	1	0	0	1	1
I/O Write (IOW)	1	0	1	1	0	1
Acknowledge of INTR (INA)	1	1	1	1	1	0
Bus Idle (BI) : DAD ACK. OF RST, TRAP HALT	0	1	0	1	1	1
	1	1	1	1	1	1
	TS	0	0	TS	TS	1

Table C-2. 80C85A Machine Cycle Chart

Machine State	Status & Buses				Control		
	S_1, S_0	$\overline{IO/\overline{M}}$	$A_8 - A_{15}$	$AD_0 - AD_7$	$\overline{RD}, \overline{WR}$	\overline{INTA}	ALE
T ₁	X	X	X	X	1	1	1 ⁽¹⁾
T ₂	X	X	X	X	X	X	0
T _{WAIT}	X	X	X	X	X	X	0
T ₃	X	X	X	X	X	X	0
T ₄	1	0 ⁽²⁾	X	TS	1	1	0
T ₅	1	0 ⁽²⁾	X	TS	1	1	0
T ₆	1	0 ⁽²⁾	X	TS	1	1	0
T _{RESET}	X	TS	TS	TS	TS	1	0
T _{HALT}	0	TS	TS	TS	TS	1	0
T _{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"

1 = Logic "1"

TS = High Impedance

X = Unspecified

Notes : (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.

(2) $\overline{IO/\overline{M}} = 1$ during T₄ – T₆ of INA machine cycle.

Table C-3. 80C85A Machine State Chart

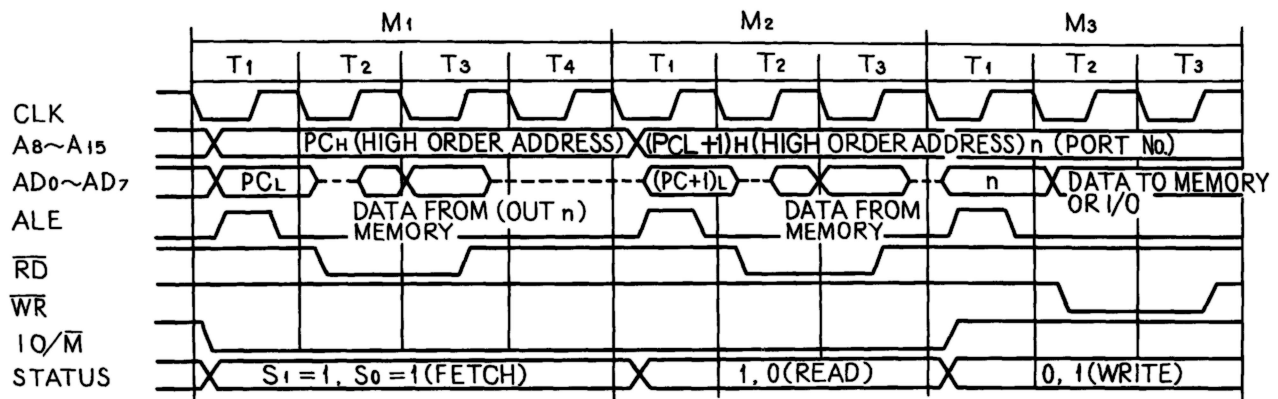


Figure C-4. 80C85A Basic System Timing

C-2. 81C55

General Description

The MSM81C55RS/GS is a 2K bit static RAM (256 byte) with parallel I/O ports. It uses silicon gate CMOS technology and consumes a standby current of 100 micro amperes maximum while the chip is not selected. Featuring a maximum access time of 400 ns, the MSM81C55RS/GS can be used in an 80C85A system without using wait states. The parallel I/O consists of two 8-bit ports and one 6-bit port (both general purpose). The MSM81C55RS/GS also contains a 14-bit programmable counter/timer which may be used for sequence-wave generation or terminal countpulsing.

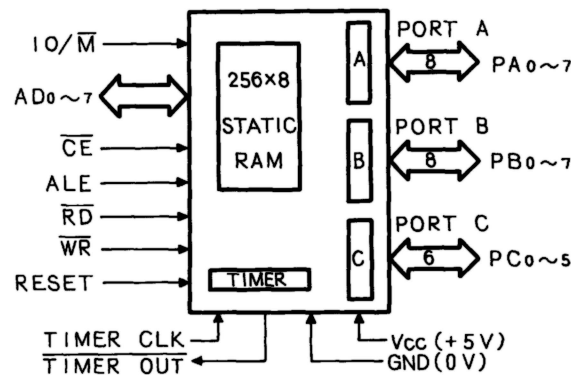


Figure C-5. Functional Block Diagram

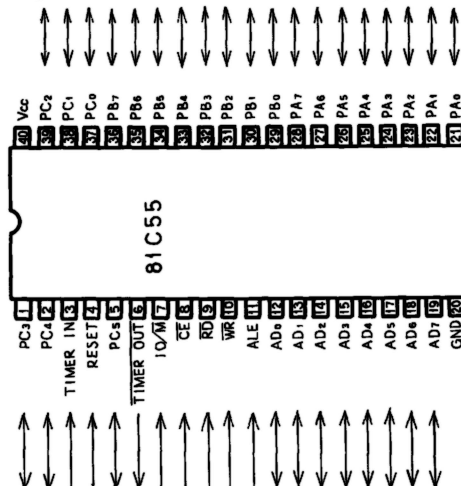


Figure C-6. Pin Configuration of 81C55

Functional Pin Description

RESET (Input)

A high level input to this pin resets the chip, placing all three I/O ports in the input mode, and stops timer.

ALE (Input)

Negative going edge of the ALE (Address Latch Enable) input latches $AD_0 \sim 7$, IO/\overline{M} , and CE signals into the respective latches.

$AD_0 \sim 7$ (Input/Output)

Three-state, bi-directional address/data bus. Eight-bit address information on this bus is read into the internal address latch at the negative-going edge of the ALE. Eight bits of data can be read from or written to the chip using this bus, depending on the state of the WRITE or READ input.

\overline{CE} (Input)

When the CE input is high, both read and write operations to the chip are disabled.

IO/\overline{M} (Input)

A high level input to this pin selects the internal I/O functions. A low level selects the memory.

\overline{RD} (Input)

If this pin is low, data from either the memory or ports is read onto the $AD_0 \sim 7$ lines, depending on the state of the IO/\overline{M} line.

\overline{WR} (Input)

If this pin is low, data on lines $AD_0 \sim 7$ is written into either the memory or into the selected port, depending on the state of the IO/\overline{M} line.

$PA_0 \sim 7$, $PB_0 \sim 7$ (Input/Output)

General-purpose I/O pins. Input/output directions can be determined by programming the command/status (C/S) register.

$PC_0 \sim 5$ (Input/Output)

Three pins are usable either as general-purpose I/O pins or control pins for the PA and PB ports. When used as control pins, they are assigned to the following functions:

PC0 : A INTR (port A interrupt)

PC1 : A BF (port A full)

PC2 : A STB (port A strobe)

PC3 : B INTR (port B interrupt)

PC4 : B BF (port B buffer full)

PC5 : B STB (port B strobe)

TIMER IN (Input)

Input to the counter/timer

$\overline{TIMER OUT}$ (Output)

Timer output. When the present count is reached during timer operation, this pin provides a square-wave or pulse output, depending on the programmed control status.

Function

81C55 has 3 functions:

- 2K bit, static RAM (256 words × 8 bits)
- Two 8-bit I/O ports (PA and PB) and a 6-bit I/O port (PC)
- 14-bit timer counter

The internal register is shown in the figure below, and the I/O addresses are described in the table following.

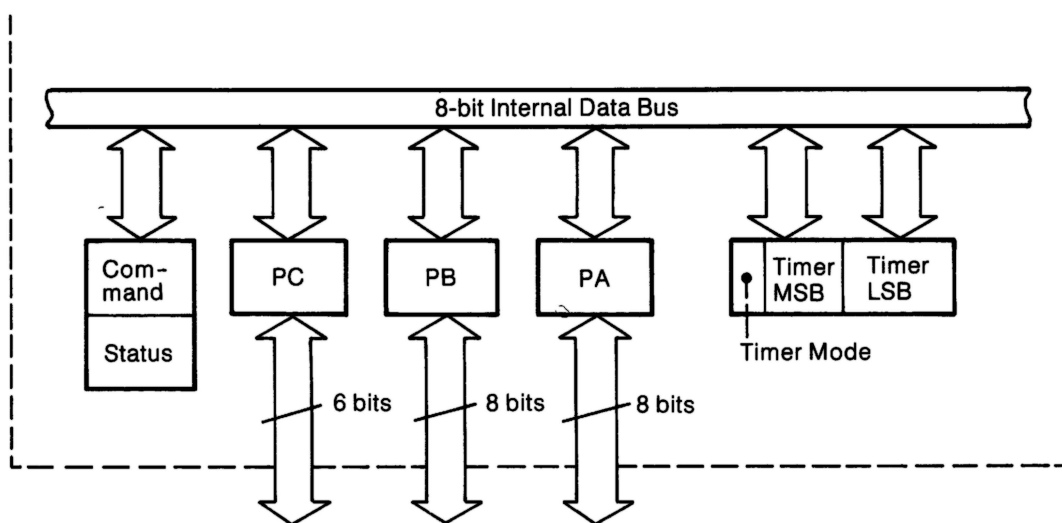


Figure C-7. Internal Register of 81C55

I/O Address								Selecting Register
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Internal command/status register
X	X	X	X	X	0	0	1	Universal I/O port A (PA)
X	X	X	X	X	0	1	0	Universal I/O port B (PB)
X	X	X	X	X	0	1	1	I/O port C (PC)
X	X	X	X	X	1	0	0	Timer count lower position 8 bits (LSB)
X	X	X	X	X	1	0	1	Timer count upper position 6 bits and timer mode 2 bits (MSB)

X : Don't care.

Table C-4. I/O Address of 81C55

(1) Programming the Command/Status (C/S) Register

The contents of the command register can be written during an I/O cycle by addressing it with an I/O address of xxxxx000. Bit assignments for the register are shown below:

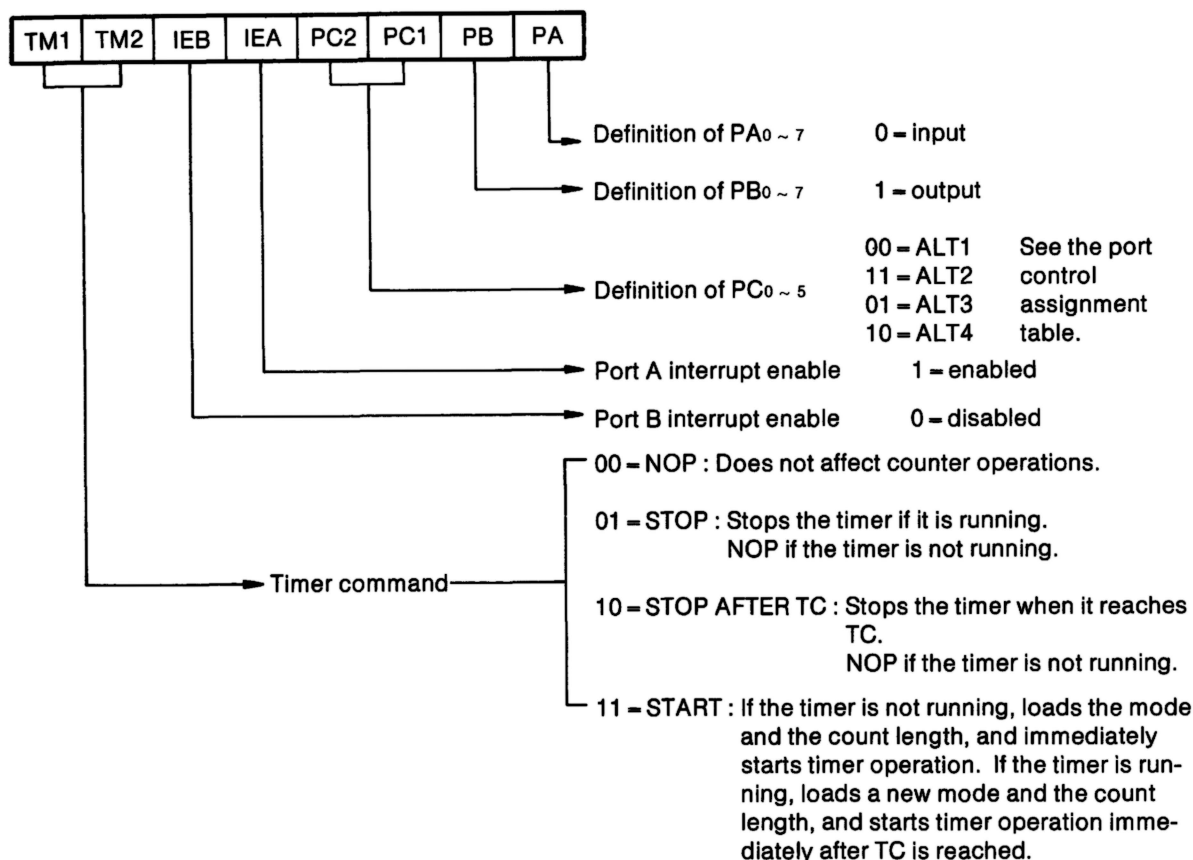


Figure C-8. Programming the Command/Status Register

Pin	ALT1	ALT2	ALT3	ALT4
PC ₀	Input port	Output port	A INTR	A INTR
PC ₁	Input port	Output port	A BF	A BF
PC ₂	Input port	Output port	A STB	A STB
PC ₃	Input port	Output port	Output port	B INTR
PC ₄	Input port	Output port	Output port	B BF
PC ₅	Input port	Output port	Output port	B STB

Table C-5. Port Control Assignment

(2) Reading the C/S Register

The I/O and timer status can be accessed by reading the contents of the Status register located at I/O address xxxxx000. The status word format is shown below:

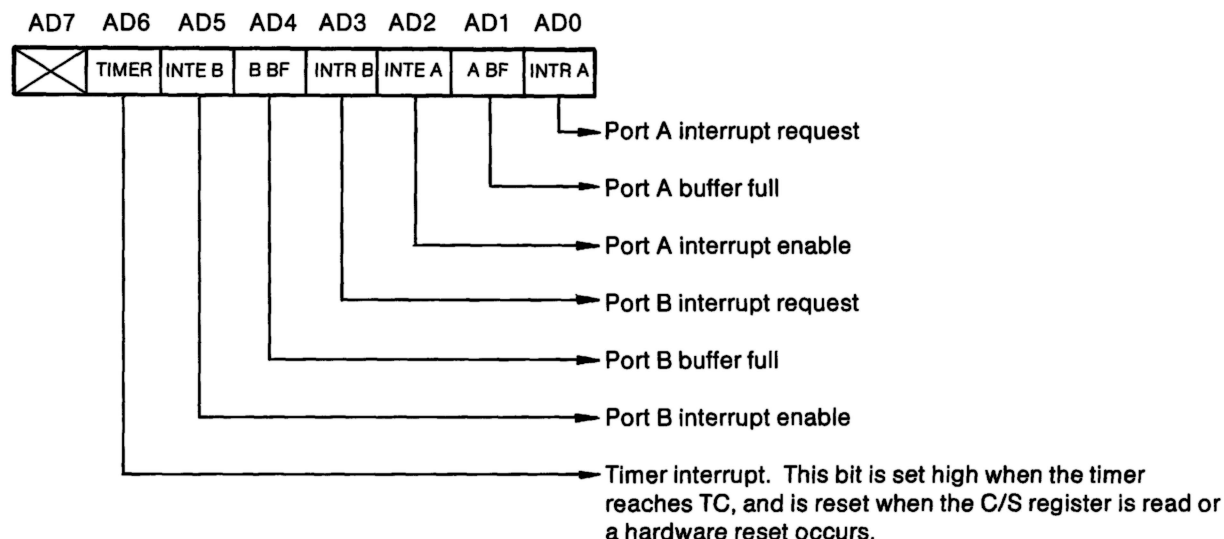


Figure C-9. Reading the C/S Register

(3) PA and PB Registers

These registers may be used as either input or output ports depending on the programmed contents of the C/S register. They may also be used either in the basic mode or in the strobe mode.

I/O address of the PA register : xxxxx001

I/O address of the PB register : xxxxx010

(4) PC Register

The PC register may be used as an input port, output port or control register depending on the programmed contents of the C/S register. The I/O address of the PC register is xxxxx011.

(5) Timer

The timer is a 14-bit counter which counts TIMER IN pulses.

The low order byte of the timer register has an I/O address of xxxxx100, and the high order byte of the register has an I/O address of xxxxx101.

The count length register (CLR) may be preset with two bytes of data. Bits 0 through 13 are assigned to the count length: bits 14 and 15 specify the timer output mode. A read operation of the CLR reads the contents of the counter and the pertinent output mode. The initial value range which can initially be loaded into the counter is 2 through 3FFF hex. Bit assignments to the timer counter and possible output modes are shown in the following.

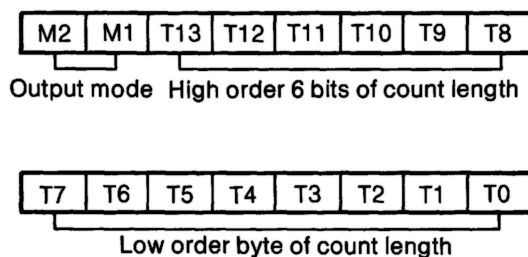


Figure C-10. Bit Assignments to the Timer Counter

M₂ M₁

- | | | |
|---|---|---|
| 0 | 0 | Outputs a low-level signal in the latter half (Note 1) of a count period. |
| 0 | 1 | Outputs a low-level signal in the latter half of a count period, automatically loads the programmed count length, and restarts counting when the TC value is reached. |
| 1 | 0 | Outputs a pulse when the TC value is reached. |
| 1 | 1 | Outputs a pulse each time the preset TC value is reached, automatically loads the programmed count length, and restarts from the beginning. |

Note 1 : When counting an asymmetrical value such as (9), a high level is output during the first period of five, and a low level is output during the second period of four.

Note 2 : If an internal counter of the 81C55 receives a reset signal, count operation stops but the counter is not set to a specific initial value or output mode. When restarting count operation after reset, the START command must be executed again through the C/S register.

(6) Standby Mode

The 81C55 is placed in standby mode when the high level at \overline{CE} input is latched during the negative-going edge of ALE. All input ports and the timer input should be pulled up or down to either Vcc or GND potential.

When using battery back-up, all ports should be set low or in input port mode. The timer output should be set low. Otherwise, a buffer should be added to the timer output and the battery should be connected to the power supply pins of the buffer.

By setting the reset input to a high level, the standby mode can be selected. In this case, the command register is reset, so the ports automatically set to the input mode and the timer stops.

C-3. 6402

General Description

The 6402 is a C-MOS LSI subsystem for interfacing the CPU to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bits code.

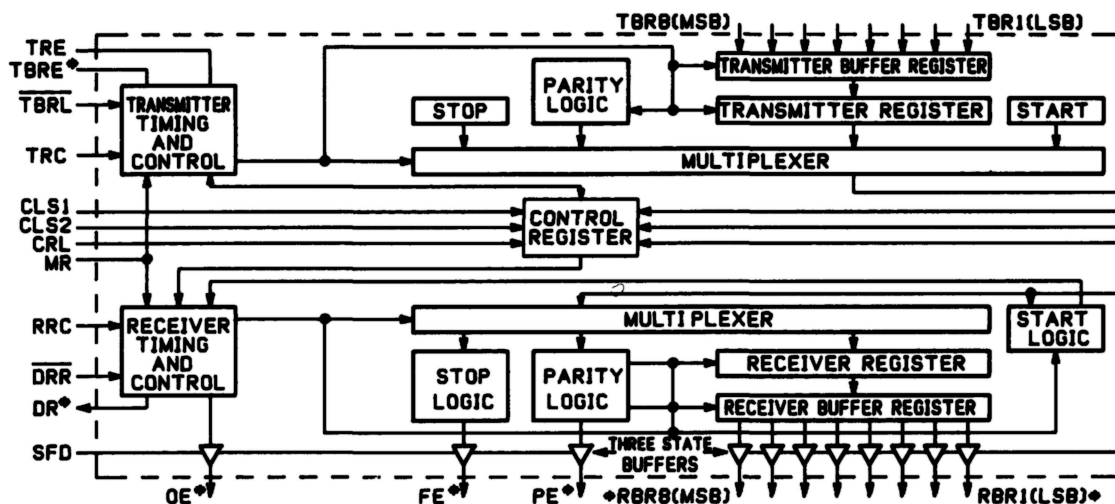


Figure C-11. Functional Block Diagram

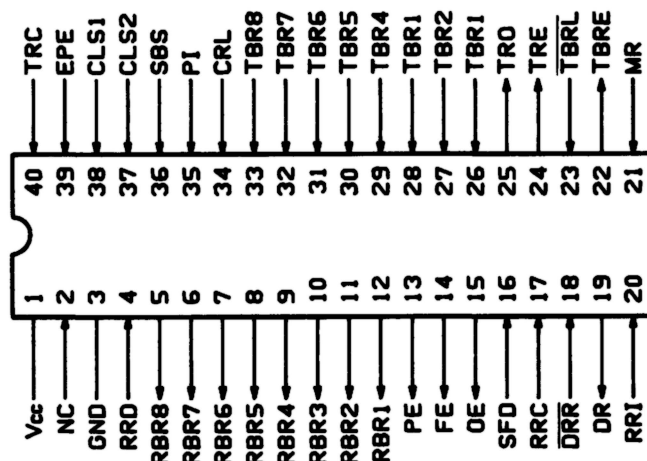


Figure C-12. Pin Configuration of 6402

Functional Pin Description

RRD (Input)

A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.

RBR1-8 (Output)

The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.

PE (Output)

A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited, this output is low.

FE (Output)

A high level on FRAMING ERROR indicates the first stop bit was invalid.

OE (Output)

A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.

SFD (Input)

A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.

RRC (Input)

The RECEIVER REGISTER CLOCK is 16X the receiver data rate.

DRR (Input)

A low level on DATA RECEIVED RESET clears the data received output DR to a low level.

DR (Output)

A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.

RRI (Input)

Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.

MR (Input)

A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up.

TBRE (Output)

A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.

TBRL (Input)

A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBRE1-8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.

TRE (Output)

A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

TRO (Output)

Character data, start and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.

TBR1-8 (Input)

Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-8. For character formats less than 8 bits the TBR8, 7 and 6 inputs are ignored corresponding to the programmed word length.

CRL (Input)

A high level on CONTROL REGISTER LOAD loads the control register.

PI (Input)

A high level on PARITY INHIBIT inhibits parity generation. Parity checking forces PE output low.

SBS (Input)

A high level on STOP BIT SELECT selects 1.5 stop bits for 5 bits character format and 2 stop bits for the other lengths.

CLS1, CLS2 (Input)

These inputs program the CHARACTER LENGTH SELECTED (CLS1 low, CLS2 low: 5 bits) (CLS1 high, CLS2 low: 6 bits) (CLS1 low, CLS2 high: 7 bits) (CLS1 high, CLS2 high: 8 bits).

EPE (Input)

When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.

TRC (Input)

The TRANSMITTER CLOCK is 16X the transmit data rate.

CONTROL WORD					DATA BITS	PARITY BIT	STOP BITS (S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

Table C-6. Control Word Format

Function

Receiver Operation

Data is received in serial form at the RRI. When no data is being received, RRI must remain high. The data is clocked through the RRC. The clock rate is 16 times the data rate.

[A] A low level on $\overline{\text{DRR}}$ clears the DR line.

[B] During the first stop bit data is transferred from the receiver register to the RBR. If the word is less than 8 bits, the unused most significant bits will be a low level. The output character is right justified to the least significant bit RBR1. A high level on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR.

[C] One clock cycle later, DR is reset to a high level and FE is evaluated. A high level on FE indicates an invalid stop bit was received, a framing error. A high level on PE indicates a parity error.

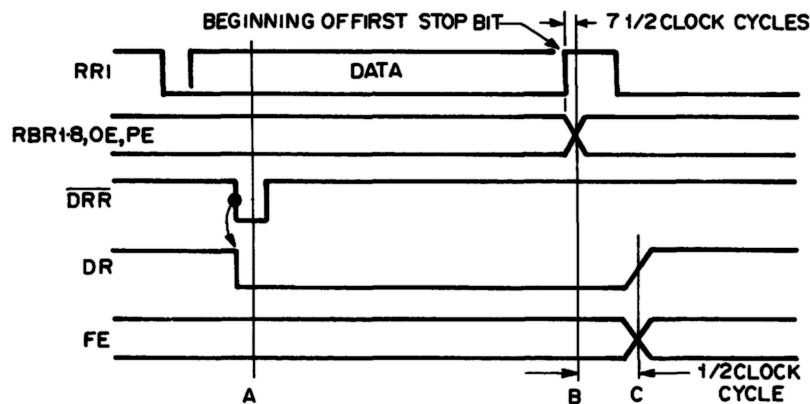


Figure C-13. Receiver Timing

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TRO terminal.

- [A] Data is loaded into the transmitter buffer register from the inputs TBR1-8 by a logic low on the $\overline{\text{TBRL}}$ input. Valid data must be present at least $t\text{-SET}$ prior to and $t\text{-HOLD}$ following the rising edge of $\overline{\text{TBRL}}$. If word less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1.
- [B] The rising edge of $\overline{\text{TBRL}}$ clears TBRE. 0 to 1 clock cycles later, data is transferred to the transmitter register, TRE is cleared, TBRE is set high, and serial data transmission is started. Output data is clocked by TRC. The clock rate is 16 times the data rate.
- [C] A second pulse on $\overline{\text{TBRL}}$ loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete.
- [D] Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.

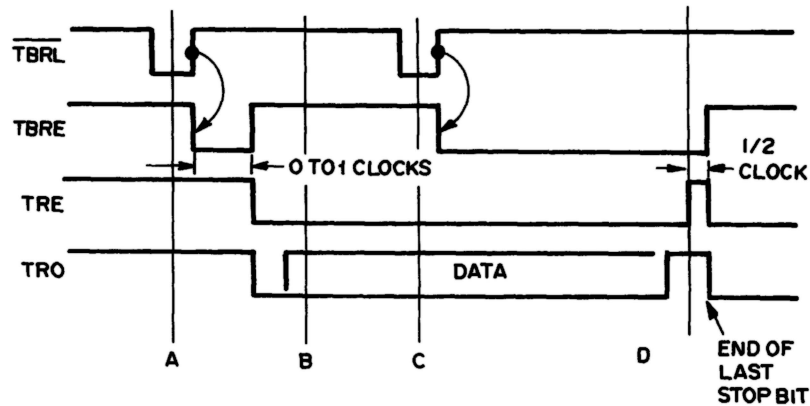


Figure C-14. Transmitter Operation

Start Bit Detection

The receiver uses a 16X clock for timing. The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7-1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within $\pm 1/2$ check cycle, $\pm 1/32$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.

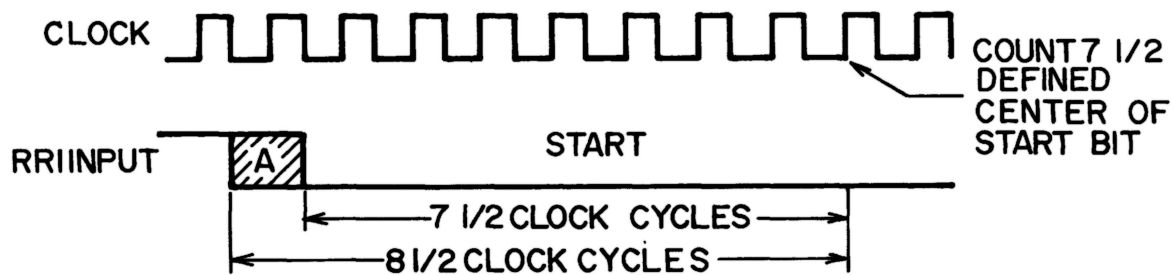


Figure C-15. Start Bit Detection Timing

C-4. Basic Construction of LCD

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical stand point, it possesses the properties of a crystal. Items which use this substance are called liquid-crystal display elements. The LCD used in the Tandy 102 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Figure C-16.

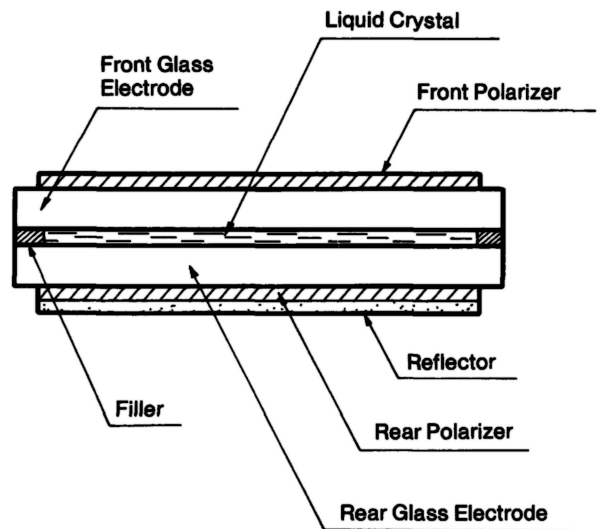


Figure C-16. Construction of LCD Panel

The LCD operates as an “electric shutter” that controls the passage of light. If voltage is applied, the transmission of light is blocked, otherwise, light is allowed to pass so that letters and numbers can be displayed.

Figure C-17 demonstrates how the LCD operates:

- The liquid-crystal display element is sandwiched between the two polarization plates. The polarized axes of the upper and lower plates are placed at right angles to each other to use the optical “twisting” of light.
- As shown in Figure C-17 (a), if voltage is not applied, the liquid-crystal molecules between the upper and lower plates twist 90° to distribute light. This results in a 90° optical movement and the transmission of light.
- In Figure C-17 (b), however, voltage is applied and the liquid appears frosted in current-carrying areas, thus blocking light transmission.

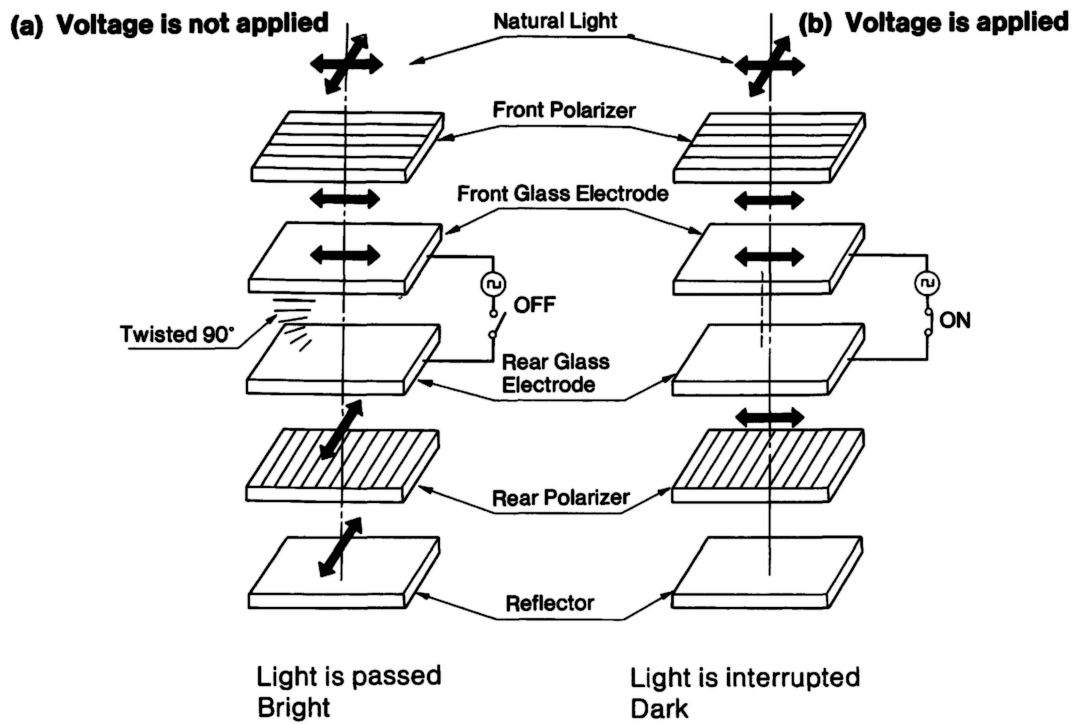


Figure C-17. Operation Theory of LCD Panel

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102

CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

AUSTRALIA

91 KURRAJONG AVENUE
MOUNT DRUITT, N S W. 2770

BELGIUM

Pare Industriel
5140 Naninne (Namur)

U K

BILSTON ROAD WEDNESBURY
WEST MIDLANDS WS10 7JN